Wideband Full-Stokes parameterized spectrometer for Xilinx RFSoC Platform

DESIGN DOCUMENT

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List of figures/tables/symbols/definitions

CASPER - Collaboration for Astronomy Signal Processing and Electronics Research

MiGen - Fragmented Hardware Description Language based in python to automate the VLSI design process.

Xilinx - FPGA manufacturer. *The FPGA used in this project is a Xilinx product.

DSP - Digital Signal Processing.

SDR - Software Defined Radio.

FPGA - Field Programmable Gate Array.

SoC - System on a Chip

1 Introduction

1.1 Acknowledgement

CASPER [1], the "Collaboration for Astronomy Signal Processing and Electronic Research" have addressed this problem by developing platform independent hardware and open source software to take advantage of developments in Field Programmable Gate Array (FPGA) and Analog to Digital Converter (ADC) technology and "quickly" target new platforms such as the Xilinx RFSoC evaluation board (ZCU111).

Xilinx University Program - Donation of the Xilinx RFSoC Eval Board.

Key Industry Consultants:

Alan Langman (Engineer @ Vermeer Corporation) - Technical guidance for Migen, CASPER, and spectrometer related material.

Dan Werthimer (Chief Scientist: SETI@Home) - Project idea, CASPER, and digital signal processing support.

Jack Hickish (Staff Researcher: UC Berkeley Radio Astronomy Lab) - CASPER, Toolflow expert, and guidance on implementation and porting

1.2 Problem and Project Statement

The problem our team will be challenged with is overhauling the CASPER Toolflow in order to allow for developers to easily become proficient in using and expanding on the existing tool set. The current toolflow prohibits new developers from making quick progress due to lack of documentation, the need for prior knowledge on MATLAB/ Simulink, and an absence of support for other FPGA platforms beyond Xilinx, such as Altera or Lattice. In doing so, our team will also develop the board support package for the Xilinx RFSoC Eval Board.

This project will work toward porting of the CASPER spectrometer instrument and its dependent libraries to the Xilinx RFSoC evaluation platform. The team will also look at improving the board support package by migrating the current tools to use Migen, an open source python library for generating and building gateware projects [2]. The team will also work on extending the toolchain to support the Xilinx Pynq infrastructure [3], which will be interfaced to the existing CASPER Python libraries.

1.3 Operational Environment

The end product will be operating within already operational server racks that are climate regulated to match manufacturer specification of optimal operating conditions including: temperature, humidity, and dust ingression. Therefore, the end product does not need to be built to work in non-common conditions due to its surrounding climate being externally controlled.

1.4 Intended Users and Uses

CASPER [1] is a community of hundreds of scientists and engineers around the world, who collaborate on the development of radio astronomy instrumentation. The CASPER community has reached out to developers to integrate Xilinx's new RFSoC platform into their current tools. Once supported, anyone making use of the open-source tools will be able to quickly develop digital instrumentation for their specific applications.

Should time allow, we will begin the next iteration of the UC Berkeley SETI Research Center's Search for Extraterrestrial Radio Emissions from Nearby Developed Intelligent Populations (SERENDIP) program [4]. This installment would be the next generation instrument system for the Search for Extraterrestrial Intelligence (SETI) coined SERENDIP VII. The system will be an open-source, ultra-high resolution, wide-bandwidth dual-pol spectrometer to be used on the world's largest radio telescopes.

1.5 Assumptions and Limitations

At this point in time, our team is assuming that basic device drivers have been developed and tested. That the CASPER spectrometer instrument will be nearly 100% compatible and operational on the Xilinx RFSoC Platform.

1.6 Expected End Product and Deliverables

Our expected deliverable is a Board Support Package for a Xilinx Zynq Ultrascale+ RFSoC evaluation board. The board support package includes porting for the CASPER spectrometer and its dependent libraries for the Xilinx board. The CASPER Toolflow is to be migrated to support Migen, an open source python library for generating and building gateware projects . It should support Xilinx Python drivers to interface with existing CASPER libraries. We must include full documentation of the implementation of the board support package. This end product is to be delivered by the end of Senior Design in May 2019.

2. Specifications and Analysis

2.1 Proposed Design

Successful creation of a Board Support Package file. This includes proper integration of the existing toolflow and any new tools to create a working Board Support Package for the Xilinx Zynq RFSoC platform. Migen will be used as the generation tool for our project which will include ensuring that it is both integrated in the current tool flow and a new tool flow of our own design.

We will need to document our process so that the open source project work can be continued by others. We also need to document our process to allow for review by the CASPER project and to give a tutorial of how our updated tool flow works. Proper documentation of our work and use of Migen is important for expanding Migen itself. We also need to document how the existing toolflow and its tools integrate with Migen.

Functional requirements:

- CASPER spectrometer support
  - The Xilinx board must be made to support the CASPER Spectrometer and the libraries it is dependent on.
- Migen
  - Migen must be able to send script to CASPER's Vivado to produce projects that the FPGA can use.
- Spectrometer
  - Parameterized inputs for user to quickly build

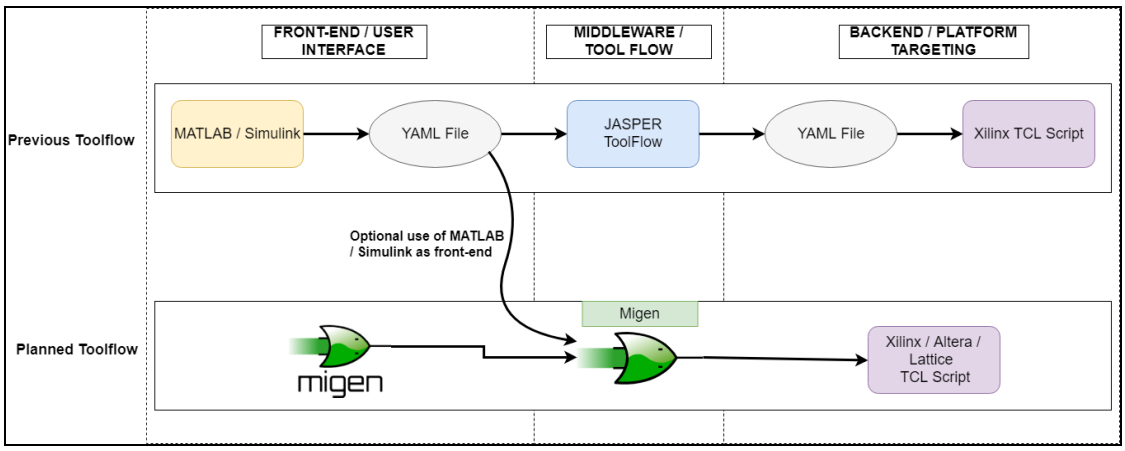
Non-Functional requirements:

- Backwards compatibility
  - The ability to STILL use MATLAB/Simulink and existing CASPER Toolflow, instead of Migen to program the board.
- Open source
  - Anyone can use our code in their application.

CASPER operates entirely under the GNU General Public License V2.0. This grants the use of the source code to anyone for commercial or private use. This also means anyone has the right to modify and/or distribute the code, however CASPER accepts no liabilities or warranties on said source code.

IEEE has several standards related to our project, since we intend this project to be used outside of our own personal use; it's important for our project to meet IEEE standards for easier use in the public domain. The IEEE Std 211-1997™ standard outlines terms and definitions that should be used when discussing Radio Wave Propagation [5]. Since, the spectrometer instrument we intend to build will interpret electromagnetic waves, any terms used to describe this instrument will adhere to this standard. The IEEE Std 1241-2010™ standard outlines terms, definitions and test methods involving Analog-to Digital Converters (ADCs) [6]. The ADC on the boards will need testing, we'll need to

ensure it is tested up to industry standards. Any references to the ADC will used this standard as a guide. The IEEE Std 802.3™ standard outlines proper protocols involved in setting up a various speeds of an Ethernet connection [7]. Our board support package requires a 10 Gbps Ethernet interface, so following the IEEE protocols for this portion of our project will help guide us to a working interface.



The specific proposed design, in Figure 1 directly above, to address our problem is to manipulate the current CASPER Toolflow and use Migen to add the ability to target various FPGA platforms as well as to ease the development of Board Support Packages. Migen can also be used as an alternative front-end to MATLAB/Simulink, removing the current toolflow's dependency on this closed-source software.

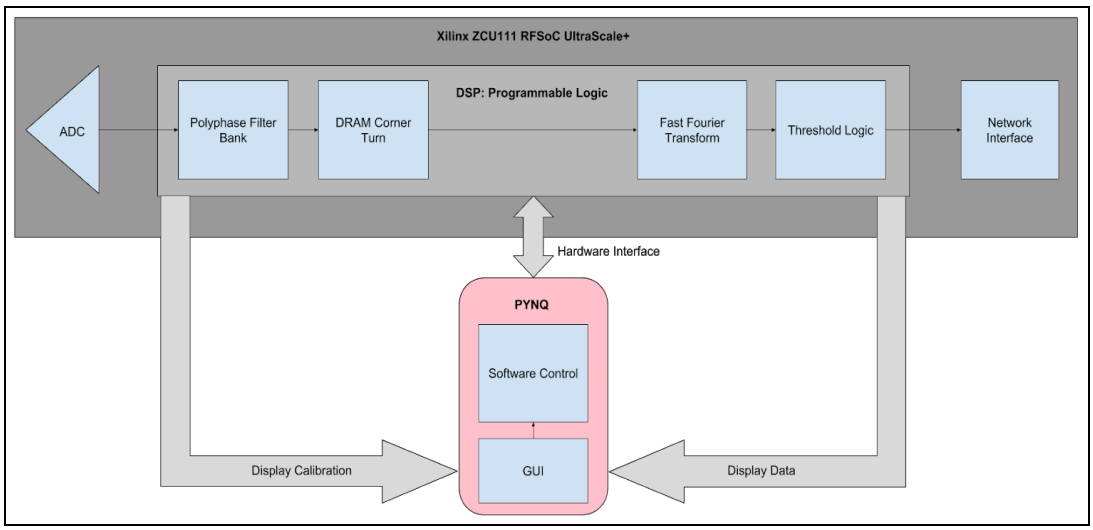


Figure 2, directly above, shows a high level functional design we are aiming to achieve for the SETI spectrometer. The four sections we can break Figure 2 into are: ADC interface, DSP logic, networking, and PYNQ software control. The DSP logic will be implemented in the CASPER Toolflow's Simulink frontend following the inner block labeled 'DSP' in Figure 2. Please refer to the "Spectrometers and Polyphase Filterbanks in Radio Astronomy" white paper for further information about the DSP design [8]. Figure 4 shows

specifically how the ethernet and networking will be implemented on board. Figure 5 depicts a block diagram of the onboard 2 Gsps ADCs via the RFSoC Data Converter IP Core.

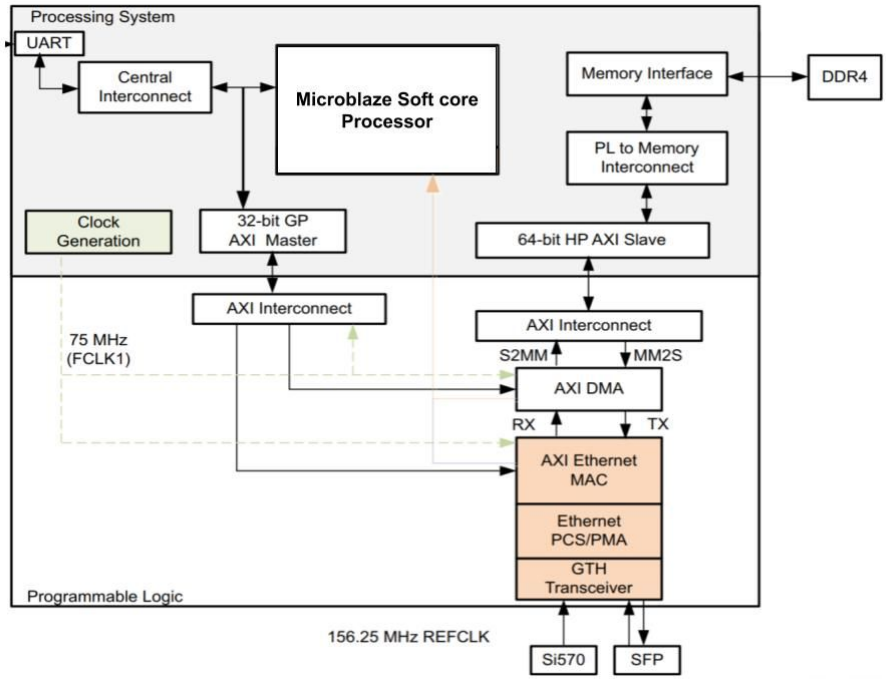


Figure 4

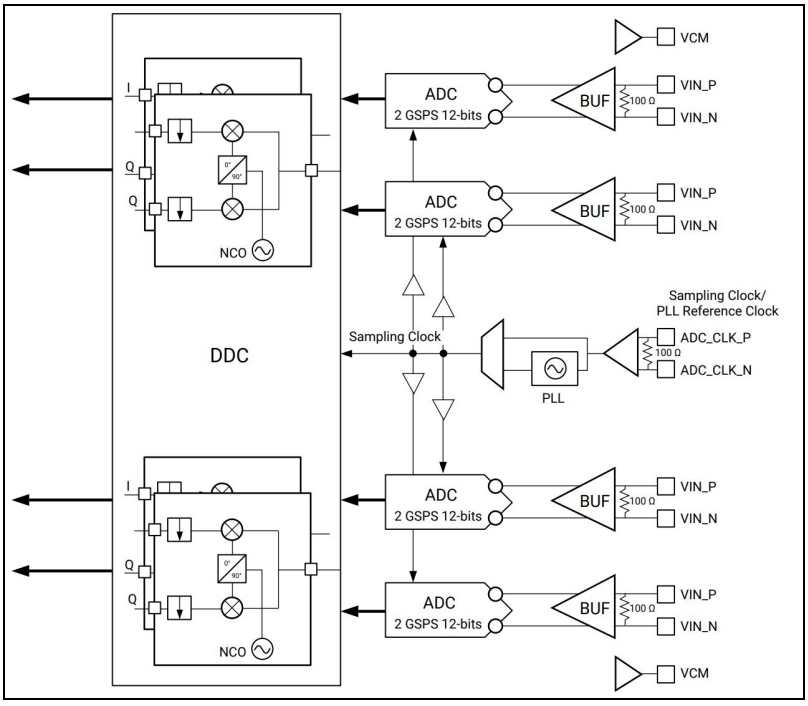


Figure 5

2.2 Design Analysis

Strengths of our proposed solution are portability, accessibility, and scalability. Using Migen as our frontend development allows for accessibility and scalability for developers because it is an open-source python library rather than a MATLAB implementation with a Python interface. Successful implementation of the toolflow using the RFSoC board will allow for greater portability because the entire system will be on a single board rather than needing separate components and interfaces. A weakness of our proposed design is the application using the board is constrained to the ADC on the board and the processing constraints of the on board processor. A trade-off of our proposed design is the use of Xilinx IP cores to implement particular functionality. This sacrifices specific functionalities of our application to be restricted to only Xilinx hardware, but increases the development time. We could alternatively have spent time implementing open-source IP cores that would have been platform agnostic, but would've taken more time to implement.

One design that we had to change from our original plans is the ethernet system. We were going to use one of the Xilinx built in implementations that uses the onboard processor to run the ethernet. This proved to be the wrong approach through discussions our team had with Key Industry Consultants. They highlighted the existing CASPER implementation of a soft core 10Gb/s ethernet implementation and to try and port that to our project. We also need to make a 1Gb/s ethernet interface using the onboard processor so that we can use PYNQ and PetaLinux with our board. It will also allow us to make our new board interface work completely separate of the data transfer interface. Beyond this we have not

currently implemented any further components of our project, but our continuing discussions with our Key Industry Consultants if any questions come up.

3 Testing and Implementation

3.1 Interface Specifications

The project will make use of many interfaces to both pass information between and validate sections of our implementation.

- PYNQ
  - PYNQ (Python Productivity for Zynq) will serve as our main interface between an external GUI (GNURadio) and the RFSoC UltraScale+ by providing a configurable data stream into and out of the FPGA platform. This tool creates an interactive window into the system which allows the user to peer into and set register values.
- GNURadio
  - GNURadio is a commonly used, open source toolkit that supplies signal processing functionality for RF hardware. This interface works in tandem with PYNQ to allow for near instantaneous interaction with the low level system of the FPGA.
- Ethernet
  - The ethernet ports onboard of the RFSoC UltraScale+ provides a hardware interface into the ZCU111. This hardware connection allows for the 10Gb/s data stream from the spectrometer instrument.
- ADC/DAC
  - ADCs (Analog-to-Digital) & DACs (Digital-to-Analog) converters allow for our system to interface with the outside world. Our project will primarily make use of the ADCs with the intent of feeding in spectrometer data for the FPGA to process. However, the project will require the use of both the ADC and DAC connectors to validate the functionality of both ports.

3.2 Hardware and software

- Hardware
  - ZCU111 - Final Development board for the project. Contains each of the necessary components on board for the CASPER project.
  - ZCU106 - Intermediate board to test preliminary Migen implementations and work out possible Migen to VIvado issues.
  - Pynq-Z1 Board - For testing purposes only, offered by Professor Jones.
- Software
  - Migen - Primary development software. Both frontend and new toolflow backend.
  - Vivado - Xilinx software that will build the output from Migen and allow for tweaks if errors are found.

- MATLAB/Simulink - Old toolflow frontend that we still plan on supporting.

To test the overall board support package we developed, we will use the CASPER Toolflow and its simple spectrometer instrument which will evaluate whether our implementation is successful. Other functional and non functional testing procuedres are listed below.

3.3 Functional Testing

The functional testings is will focus on the 1Gb/s ethernet interface, since the speed of transfer does not need to be consistently fast at a certain rate. UDP packets and proper DHCP for the interface will be checked up to standard IEEE Std 802.3 [7]. To test the ADC functionality we will follow section 4 of IEEE Std 1241™-2010 [6]. This standard provides both procedure and result for testing ADC's that we will use as reference when we test ours. To test the overall board support package we developed, we will use the CASPER Toolflow and its simple spectrometer instrument which will evaluate whether our implementation is successful. The simple spectrometer instrument will evaluate our implementation by operating within the specified constraints of the toolflow as designed by the CASPER organization.

3.4 Non-Functional Testing

We will test that the 10Gb/s ethernet interface is able to transfer 128 byte UDP packets at 98% baud rate consistently for an hour. Testing udp packets and proper DHCP up to standard IEEE Std 802.3 [7]. Test the accuracy of the DSP data flow and calibration of the ADC. We will also have to benchmark the performance of the 1 gigabit ethernet core and the potential 10Gb/s. We will be testing the compatibility of the Migen code we develop with the old toolflow. We also need to test the usability of our interface for the new toolflow.

3.5 Process

We described above how we will approach testing in the future, however at this point we are only starting the implementation phase of our project, so we are unable to elaborate on the how each method has been tested.

3.6 Results

At this point we are starting the implementation phase of the project, so we are unable to elaborate on results.

4 Closing Material

4.1 Conclusion

So far we have successfully created platform files in Migen to begin porting of an existing CASPER spectrometer project. We have also investigated the proper implementation of ethernet and have found Xilinx documentation for the Ultrascale+ architecture to successfully implement a 1Gb/s interface. We will also be porting the existing programmable logic and Microblaze softcore processor implementation of CASPER's 10Gb/s interface. Our goals are to successfully complete a new branch of the CASPER Toolflow that still supports the existing toolflow. We achieve this through the use of Migen, PYNQ, PetaLinux, and GNURadio. The final goal is then to complete a successful implementation of a spectrometer within CASPER specifications using the newly developed toolflow on the ZCU111 board that integrates previously separate components on one board. We believe that using Migen as the backend to our project is the best course of action because it provides great flexibility in board and component choice and allows for development using fully open source software whereas the previous toolflow required use of MATLAB, which is a proprietary software.

4.2 References

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6. IEEE Std 1241-2010™ IEEE Standard of Terminology and Test Methods for Analog-to Digital Converters

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8. Price, D. (2018). Spectrometers and Polyphase Filterbanks in Radio Astronomy. [online] Arxiv.org. Available at: https://arxiv.org/abs/1607.03579 [Accessed 23 Oct.

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10. Xilinx.com. (2018). *Zynq UltraScale+ RFSoC Data Converter*. [online] Available at: https://www.xilinx.com/support/documentation/ip_documentation/usp_rf_data_converter/v2_0/pg269-rf-data-converter.pdf [Accessed 23 Oct. 2018].

4.3 Appendices

[1] ZCU111 User Guide - https://www.xilinx.com/support/documentation/boards_and_kits/zcu111/ug1271-zcu111-eval-bd.pdf

[2] Petalinux User Guide - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2018_2/ug1144-petalinux-tools-reference-guide.pdf