Wideband Full-Stokes parameterized spectrometer for Xilinx RFSoC Platform

PROJECT PLAN

Team 41
Professor Phillip Jones
Advisers
Team Members/Roles
Brian Bradford
Vishal Joel
Jared Danner
Louis Hamilton
Nick Knuth
Team Email
sdmay19-41@iastate.edu
Team Website
sdmay19-41.sd.ece.iastate.edu

Revised: 11/27/2018/#3.0

Table of Contents

List of Figures

List of Tables

List of Definitions

CASPER - Collaboration for Astronomy Signal Processing and Electronics Research

MiGen - Fragmented Hardware Description Language based in python to automate the VLSI design process.

Xilinx - FPGA manufacturer. *The FPGA used in this project is a Xilinx product.

DSP - Digital Signal Processing

FPGA - Field Programmable Gate Array

SoC - System on a Chip

PYNQ - Python productivity for Zynq platforms

IP core - Intellectual Property core

casperfpga - a python library used to interact and interface with CASPER Hardware. Functionality includes being able to reconfigure firmware, as well as read and write registers across the various communication interfaces.

1 Introductory Material

1.1 Acknowledgement

CASPER [1], the “Collaboration for Astronomy Signal Processing and Electronic Research” have addressed this problem by developing platform independent hardware and open source software to take advantage of developments in Field Programmable Gate Array (FPGA) and Analog to Digital Converter (ADC) technology and “quickly” target new platforms such as the Xilinx RFSoC evaluation board (ZCU111).

Xilinx University Program - Donation of the Xilinx RFSoC Eval Board.

Key Industry Consultants:

Alan Langman (Engineer @ Vermeer Corporation) - Technical guidance for Migen, CASPER, and spectrometer related material.

Dan Werthimer (Chief Scientist: SETI@Home) - Project idea, CASPER, and digital signal processing support.

Jack Hickish (Staff Researcher: UC Berkeley Radio Astronomy Lab) - CASPER, Toolflow expert, and guidance on implementation and porting

1.2 Problem Statement

The problem our team will be challenged with is overhauling the CASPER Toolflow in order to allow for developers to easily become proficient in using and expanding on the existing tool set. The current toolflow prohibits new developers from making quick progress due to lack of documentation, the need for prior knowledge on MATLAB / Simulink, and an absence of support for other FPGA platforms beyond Xilinx, such as Altera or Lattice. In doing so, our team will also develop the board support package for the Xilinx RFSoC Eval Board.

This project will work toward porting of the CASPER spectrometer instrument and its dependent libraries to the Xilinx RFSoC evaluation platform. Using the RFSoC allows for the ADC, DAC, processor, and networking to all be on a single board rather than needing separate components and interfaces for each. The team will also look at improving the board support package by migrating the current tools to use Migen, an open source python library for generating and building gateware projects [2]. The ultimate goal of the new toolflow, which incorporates support for Migen and PYNQ, is to make FPGA programming easier so that researchers/developers can quickly develop instrumentation to meet their scientific requirements. The team will also work on extending the toolchain to support the Xilinx PYNQ infrastructure [3], which will be interfaced to the existing CASPER Python libraries.

1.3 Operating Environment

The end product will be operating within already operational server racks that are climate regulated to match manufacturer specification of optimal operating conditions including: temperature, humidity, and dust ingression. Therefore, the end product does not need to be built to work in non-common conditions due to its surrounding climate being externally controlled.

1.4 Intended Users and Intended Uses

CASPER [1] is a community of hundreds of scientists and engineers around the world, who collaborate on the development of radio astronomy instrumentation. The CASPER community has reached out to developers to integrate Xilinx's new RFSoC platform into their current tools. Once supported, anyone making use of the open-source tools will be able to quickly develop digital instrumentation for their specific applications.

Should time allow, we will begin the next iteration of the UC Berkeley SETI Research Center's Search for Extraterrestrial Radio Emissions from Nearby Developed Intelligent Populations (SERENDIP) program [4]. This installment would be the next generation instrument system for the Search for Extraterrestrial Intelligence (SETI) coined SERENDIP VII. The system will be an open-source, ultra-high resolution, wide-bandwidth dual-pol spectrometer to be used on the world's largest radio telescopes.

1.5 Assumptions and Limitations

At this point in time, our team is assuming that basic device drivers have been developed and tested. That the CASPER spectrometer instrument will be nearly 100% compatible and operational on the Xilinx RFSoC Platform.

1.6 Expected End Product and Other Deliverables

Our expected deliverable is a Board Support Package for a Xilinx Zynq Ultrascale+ RFSoC evaluation board. The board support package includes porting for the CASPER spectrometer and its dependent libraries for the Xilinx board. The CASPER Toolflow is to be migrated to support Migen, an open source python library for generating and building gateware projects . It should support Xilinx Python drivers to interface with existing CASPER libraries. We must include full documentation of the implementation of the board support package. This end product is to be delivered by the end of Senior Design in May 2019.

2 Proposed Approach and Statement of Work

2.1 Objective of the Task

Expected tasks:

1. Porting of the CASPER spectrometer instrument and dependent libraries to the Xilinx ZCU111 evaluation platform.
    a. General board support
    b. Ethernet interface
    c. ADC interface
2. Migrating the current CASPER Toolflow to use Migen, an open source python library for generating and building gateware projects.
3. Support for Xilinx PYNQ infrastructure, which will interface to existing CASPER Python libraries.
4. Documentation of project for future users: source code, gateware, and firmware descriptions.

Additional task:

1. Wideband full stokes parameterized spectrometer (polarimeter) for radio astronomy applications, targeting the Xilinx Zynq RFSoC platform.

2.2 Functional Requirements

Successful creation of a Board Support Package file. This includes proper integration of the existing toolflow and any new tools to create a working Board Support Package for the Xilinx Zynq RFSoC platform. Migen will be used as the generation tool for our project which will include ensuring that it is both integrated in the current tool flow and a new tool flow of our own design.

Proper documentation of process. We will need to document our process so that the open source project work can be continued by others. We also need to document our process to allow for review by the CASPER community and to give a tutorial of how our updated toolflow works.

Proper documentation of tools used. Proper documentation of our work and use of Migen is important for expanding Migen itself. We also need to document how the existing toolflow and its tools integrate with Migen.

2.3 Constraints Considerations

- Functional
    - CASPER spectrometer support
        - The Xilinx board must be made to support the CASPER spectrometer and the libraries it is dependent on.
    - Migen
        - Migen must be able to send script to CASPER's Vivado to produce projects that the FPGA can use.
    - Spectrometer
        - Parameterized inputs for user to quickly build
- Non-Functional
    - Backwards compatibility
        - The ability to STILL use MATLAB/Simulink and existing CASPER Toolflow, instead of Migen to program the board.
    - Open source
        - Anyone can use our code in their application.
    - IEEE
        - Standard Definitions of Terms for Radio Wave Propagation
        - Standard of Terminology and Test Methods for Analog-to Digital Converters
        - Standards for Ethernet

CASPER operates entirely under the GNU General Public License V2.0. This grants the use of the source code to anyone for commercial or private use. This also means anyone has the right to modify and/or distribute the code, however CASPER accepts no liabilities or warranties on said source code.

CASPER has a stated code of conduct, as part of working with CASPER we must adhere to the policies outlined in this document [5]. Otherwise, we'll adhere Iowa State ECE's lab safety procedures outlined by ECpE Lab Safety Procedures [6]. This mostly ensures no unintentional damage is done to lab equipment and individuals present in the lab. The boards that we are working with are costly and proper lab procedures will ensure there are minimal chances for damaging the boards.

IEEE has several standards related to our project, since we intend this project to be used outside of our own personal use; it's important for our project to meet IEEE standards for easier use in the public domain. The IEEE Std 211-1997™ standard outlines terms and definitions that should be used when discussing Radio Wave Propagation [7]. Since, the spectrometer instrument we intend to build will interpret electromagnetic waves, any terms used to describe this instrument will adhere to this standard. The IEEE Std 1241-2010™ standard outlines terms, definitions and test methods involving Analog-to Digital Converters (ADCs) [8]. The ADC on the boards will need testing, we'll need to ensure it is tested up to industry standards. Any references to the ADC will used this standard as a guide. The IEEE Std 802.3™ standard outlines proper protocols involved in setting up a various speeds of an Ethernet connection [9]. Our board support package

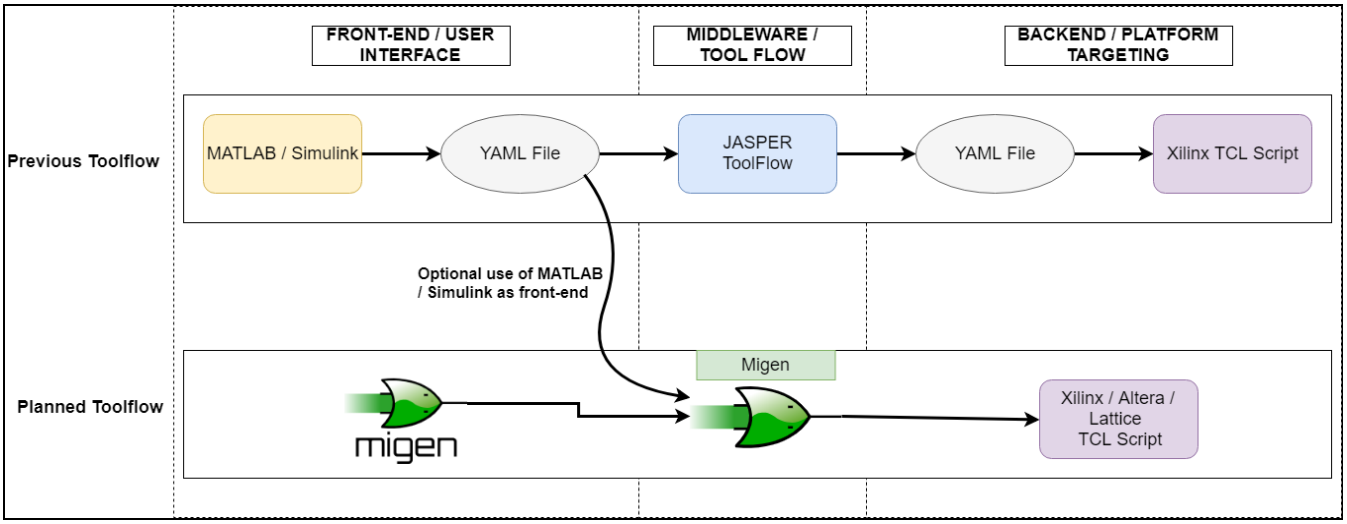
requires a 10 Gbps Ethernet interface, so following the IEEE protocols for this portion of our project will help guide us to a working interface.

2.4 Previous Work And Literature

Two previous CASPER Toolflow board support projects were completed in past two years by the South African Radio Astronomy Observatory's (SARAO) support for the SKARAB board [10], and the Institute of Automation, Chinese Academy of Sciences support for the SNAP2 board [11]. In both cases a Microblaze softcore processor was used as a system controller. This softcore processor is currently implemented in the FPGA fabric/programmable logic. We can now take advantage of the hardcore ARM processor on board as the system controller with the Zynq architecture and port the existing Microblaze code to run on ARM. In both cases a python library called *casperfpga* is used to interface with the board, which requires a steep learning curve for new developers. Instead, we will leverage PYNQ support of the Zynq architecture to achieve the same functionality requiring less development time.

Should we complete the Board Support Package before the end of Senior Design, we will attempt to implement the next generation SETI spectrometer: SERENDIP VII. This would be the next iteration of this application, the prior was SERENDIP VI [4]. It would be an improvement by both bandwidth and spectral resolution.

2.5 Proposed Design



The proposed design, in Figure 1 directly above, to address our problem is to manipulate the current CASPER Toolflow and use Migen to add the ability to target various FPGA platforms as well as to ease the development of Board Support Packages. Migen can also be used as an alternative front-end to MATLAB/Simulink, removing the current toolflow's dependency on this closed-source software.

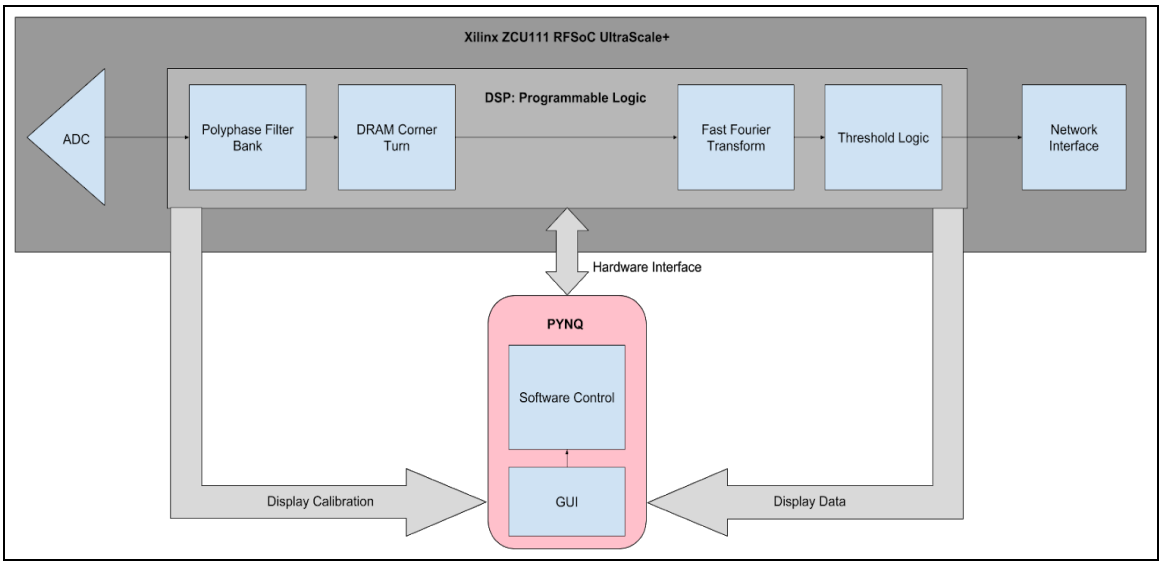


Figure 2, directly above, shows a high level functional design we are aiming to achieve for the SETI spectrometer. The four sections we can break Figure 2 into are: ADC interface, DSP logic, networking, and PYNQ software control. The DSP logic will be implemented in the CASPER Toolflow's Simulink frontend following the inner block labeled 'DSP' in Figure 2. Please refer to the "Spectrometers and Polyphase Filterbanks in Radio Astronomy" white paper for further information about the DSP design [14]. Figure 4 shows specifically how the ethernet and networking will be implemented on board. Figure 5 depicts a block diagram of the onboard 2 Gsps ADCs via the RFSoC Data Converter IP Core.

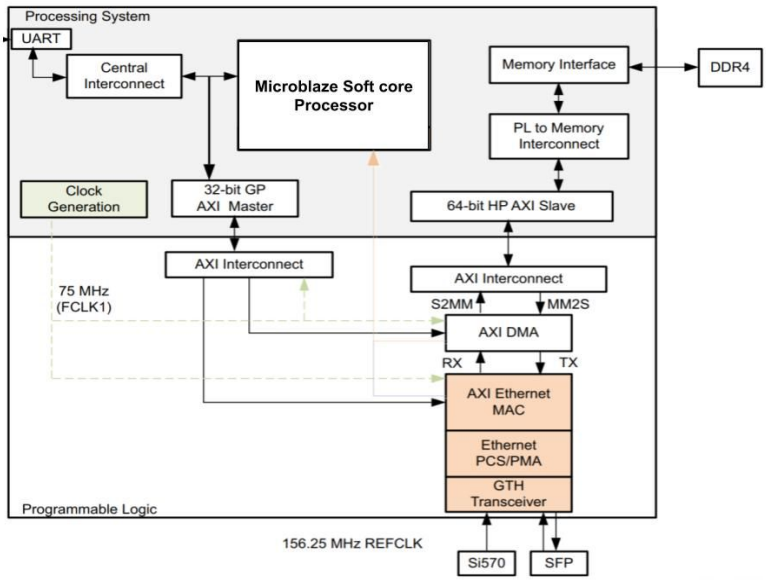


Figure 4

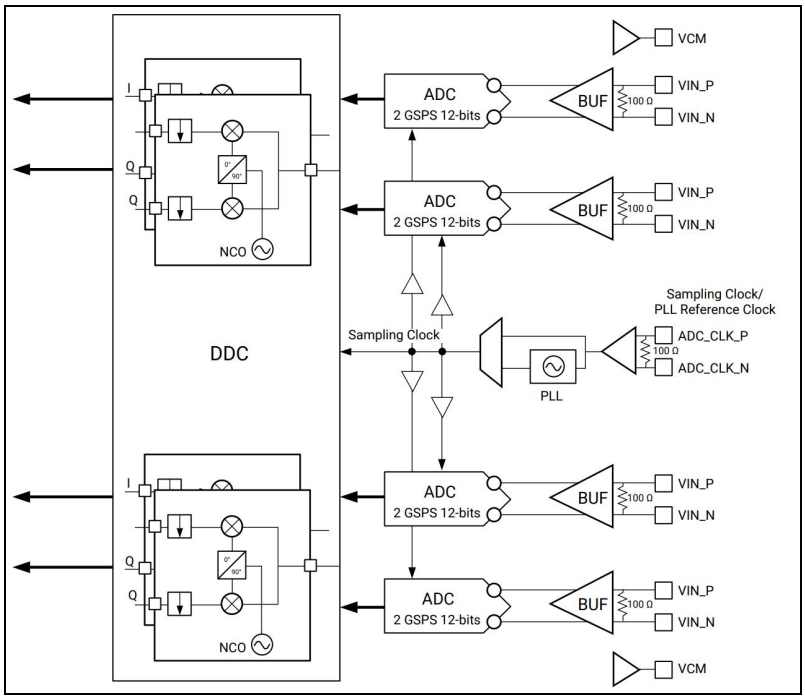


Figure 5

Strengths of our proposed solution are portability, accessibility, and scalability. Using Migen as our frontend development allows for accessibility and scalability for developers because it is an open-source python library rather than a MATLAB implementation with a Python interface. Successful implementation of the toolflow using the RFSoC board will allow for greater portability because the entire system will be on a single board rather than needing separate components and interfaces. A weakness of our proposed design is the application using the board is constrained to the ADC on the board and the processing constraints of the on board processor. A trade-off of our proposed design is the use of Xilinx IP cores to implement particular functionality. This sacrifices specific functionalities of our application to be restricted to only Xilinx hardware, but increases the development time. We could alternatively have spent time implementing open-source IP cores that would have been platform agnostic, but would've taken more time to implement.

2.6 Technology Considerations

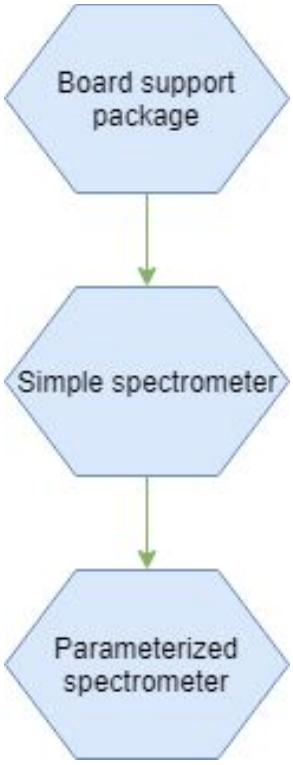
If successful in implementation, this would be the first Zynq SoC board to be integrated in the tool flow allowing for the board to run everything rather than needing auxiliary components. Using Migen should allow the toolflow to be ported completely to python removing the need for MATLAB and the current clunky python implementation while maintaining backwards compatibility with the MATLAB tools. A weakness of the technology being used is the heavy reliance on Migen and the potential for it not to work.

A trade off of having a SoC is that we are constrained to the components on board such as the ADC and processor.

2.7 Safety Considerations

We must obey all posted signs and warnings as well as instructions issued by the lab instructor in the laboratory. We must know the location of the fire extinguishers, First Aid kits and their proper use. The improper or unsafe use of laboratory equipment is potentially dangerous. Therefore, we must not use lab equipment for purposes other than this class' work. We must understand the emergency shutdown procedures (when necessary) for any lab equipment that we are using. We must understand and comply with electrical safety procedures.

2.8 Task Approach



This diagram displays a basic approach towards our proposed project timeline. With the first phase, we begin with the board support package starting with the creation of a platform python file in Migen for both the ZCU106/111 that will link FPGA pins to Python object signals to be manipulated by Migen. We will then create PYNQ images for both the ZCU106/111 that will support DisplayPort and HDMI, User LEDs/switches/push buttons, Pmod, and 1 GbE ethernet interface. Finally for this phase, we will port an existing 10GbE core from the CASPER Toolflow to Migen to work with the ZCU111 board.

For the second phase, we shift towards implementing a simple spectrometer beginning with a working ADC core that interfaces with the high-speed ADC's on the ZCU111. Next, we will create a fork within the current CASPER Toolflow to support Migen for the ZCU111. Future users will then be able to decide whether they prefer a MATLAB or Migen frontend for development. To conclude this phase, we will add backwards-compatibility with casperfpga (the current way of interfacing with an FPGA via an ethernet link) via wrapping PYNQ, which matches the same functionality.

Finally, the parameterized spectrometer phase of this project will involve the implementation of DSP logic using existing CASPER Toolflow blocks including a Polyphase Filterbank, DRAM Corner Turner, FFT algorithm, and thresholding logic block to finally output the data over a 10GbE ethernet link. In addition, this phase will include the creation of a GNURadio, python-based GUI that will allow the user of the spectrometer to view particular data in real-time and tweak parameters accordingly via PYNQ overlays that will be created for the ADC and DSP programmable logic.

2.9 Possible Risks And Risk Management

- Completely new concept - There isn't any other Zynq Soc-type platform that supported within the CASPER's community. So overall, the whole project implementation is fairly new.
- Lack of documentation on Migen - Migen's documentation is quite lacking. Their documentation offers the bare minimum assistance required to set up the tool, but when it comes to our project implementation a lot of research will need to be done to get it up and working.
- New to the project members - Most of the team members are fairly new to working with FPGA boards, at least at this level. Therefore there is a big learning curve that needs to be addressed.

2.10 Project Proposed Milestones and Evaluation Criteria

Milestones:

- Getting around the dependency on MATLAB/Simulink while not completely eliminating the backward compatibility with these tools.
- Reliable documentation and open source tools, gateware, firmware descriptions that may gain attention from other developers.
- Open source tools that may help with support for other FPGA platforms.

2.11 Project Tracking Procedures

Our group will make use of the Issue Board included with our Iowa State GitLab repository. This is a project management tool that can be used to plan, organize, and visualize our workflow towards tasks involved with our project. We will also keep an eye on the activity metrics that are tracked by GitLab. The Wiki Board will be used to document things as we progress through our project.

2.12 Expected Results and Validation

Our desired outcome would be the Xilinx RFSoC board fully supported within the current CASPER Toolflow as well as Migen. We will validate the functionality of the ethernet interface by both echoing UDP packets through the interface and ensuring the board will DHCP correctly to obtain an IP address. We will validate the functionality of ADC interface by generating a signal in the lab and ensuring that the ADC digitizes the signal correctly. We will validate the general board support within the CASPER Toolflow and Migen by compiling the CASPER Wideband Spectrometer tutorial for our board. This tutorial design also incorporates both the Ethernet and ADC interfaces as well as DSP logic which will demonstrate programmable logic and processing system board support.

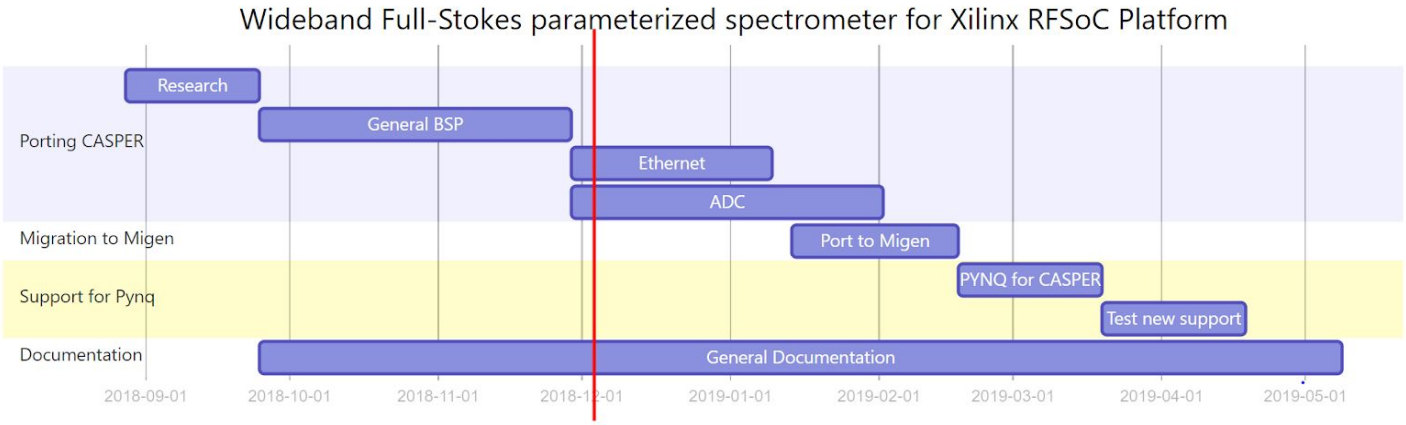
2.13 Test Plan

We will test that the 10Gb/s ethernet interface is able to transfer 128 byte udp packets at 98% baud rate consistently for an hour. For the 1Gb/s ethernet interface, our main testing

will be focused on functionality because the speed of transfer does not need to be consistently fast at a certain rate. We will test udp packets and proper DHCP for both interfaces. The 10Gb/s interface will be implemented entirely in programmable logic using a microblaze soft core while the 1Gb/s interface will use the on board processor and our linux installation. To test the ADC functionality we will follow section 4 of IEEE Std 1241™-2010 [12]. This standard provides both procedure and result for testing ADC's that we will use as reference when we test ours. To test the overall board support package we developed, we will use the CASPER Toolflow and its simple spectrometer instrument which will evaluate whether our implementation is successful. The simple spectrometer instrument will evaluate our implementation by operating within the specified constraints of the toolflow as designed by the CASPER organization.

3 Project Timeline, Estimated Resources, and Challenges

3.1 Project Timeline



This gantt chart is based off of the tasks listed in section 2.1. The gap in the middle is the break between semesters. The first main section is doing an initial port of the current toolflow to the new board we will be using. This is so that we can integrate the new architecture of a SoC into the existing toolflow and find any issues with the new architecture quickly. The substeps within this section are researching the CASPER project and its current toolflow. The next section is developing a basic board support package for the new board to learn its architecture. The next step will be including networking support through the use of the on board ethernet port. The final step in this section will be adding the ADC interface and the DSP logic. This section should result in a successful port of the current toolflow to the new board. The next section will be writing Migen libraries to support the new board's architecture and the current toolflow's front end system. The final section will be developing a support package for the PYNQ libraries

available for the board and use them along with Migen as a new interface in the toolflow. The first substep in this section will be looking at PYNQ's capabilities and configuring it for the CASPER Toolflow. The next step will be testing this implementation and the overall implementation of the project as a whole. Throughout the semester there will be documentation work as shown by the final section.

3.2 Feasibility Assessment

Our project group, client, and advisor have assessed the required tasks needed complete the overall goal and we have concluded that it will be difficult, but doable if given the proper amount of time and effort.

Some foreseen challenges that our group has accounted for are: the variable scope of the supported libraries already created for our desired Xilinx platform (board support package), getting the required hardware to achieve meaningful testing, and our assumption that Migen will work as specified and not cause any unforeseen problems.

To mitigate some of the foreseen challenges we are trying to keep our approach in Migen and supporting libraries as general as possible so that we can take another route if we need to. We are also attempting to use as much prior work as possible to avoid potential pitfalls of redoing work that is already done in the CASPER Toolflow. Two of our team members have and continue to work closely with other professionals working on the CASPER Toolflow and have access to their guidance and will be working with them directly to get a better understanding of the approach we are taking.

3.3 Personnel Effort Requirements

Task	Expected Effort in hours
Porting CASPER spectrometer to ZCU111 with Migen and new toolflow	75
Migrating CASPER Toolflow to Migen	150
PYNQ and GNURadio support	90
Documentation	100
Simple Spectrometer	40

We believe that the first task of implementing the CASPER spectrometer should only take approximately 75 hours. This task should take this amount because all we are doing in this task is taking an existing project and recreating it in Migen. This includes rewriting the

code in python using Migen and testing the implementation to make sure we have Migen configured properly.

The second task of migrating the current toolflow to Migen is a much larger undertaking. This task will be translating the current Matlab frontend implementation so that it will work with Migen. It also includes developing a Migen only frontend that can be used as a secondary new toolflow. This is a large task as rather than translating a single project to the new toolflow we need to implement scripts to handle translation and direct implementation of the existing CASPER components. We expect this task to take double the time of a single project implementation because of the scope of the work needed which mean approximately 150 hours

The third task labeled "PYNQ and GNURadio support", which consists of 1) understanding how GNURadio and PYNQ can work in tandem 2) modifying GNURadio's well adopted interface to make use of a data stream that will be provided by PYNQ, and 3) correctly using the new system to calibrate & display the information being transferred to and from the RFSoC UltraScale+ Platform. We have estimated that, based off our current knowledge, this subset of tasks will take our team approximately 90 hours to implement and fine tune before it is in a successful state.

The fourth task of documentation is expected to take approximately 100 hours over the rest of the project. We believe it will take this long because we will need to document not only the code we write, but how to use the new toolflow. This will include a lot of wiki style documentation and tutorials along with a set of well structured code references. We will also need to complete proper documentation for the senior design class.

The last major task is porting CASPER's Simple Spectrometer Instrument to make use of Migen instead of MATLAB/VHDL backend code. We plan for this task to take considerably less time than the others due to our future knowledge that we will have gained from porting both the RFSoC (ZCU111) and the CASTER Toolflow. This task will be the final test of our entire project to ensure that all prior pieces are working optimally and that Migen will be able to handle all the jobs needed by the CASPER organization.

3.4 Other Resource Requirements

- Xilinx Zynq Ultrascale+ RFSoC evaluation board.
- Xilinx Platform II Cable.
- Access to the ISU ECPE linux servers and their tools.

3.5 Financial Requirements

There is no current foreseen financial resources required for this project given that the Xilinx University Program donates the Xilinx Zynq RFSoC board for our project.

4 Closure Materials

4.1 Conclusion

The problem our team will be challenged with is overhauling the CASPER Toolflow in order to allow for developers to easily become proficient in using and expanding on the existing tool set. In doing so, our team will also continue development of the board support package for the Xilinx RFSoC Eval Board.

The stated problem is a necessary task that, when completed, will ensure that the CASPER organization is well equipped and able to continue its development into the future on a solid foundation.

4.2 References

1. Casper-dsp.org. (2018). *The Collaboration for Astronomy Signal Processing and Electronics Research*. [online] Available at: http://casper-dsp.org/ [Accessed 23 Oct. 2018].

2. M-labs.hk. (2018). *Migen | M-Labs*. [online] Available at: https://m-labs.hk/migen/index.html [Accessed 23 Oct. 2018].

3. Readthedocs.org. (2018). *PYNQ | Read the Docs*. [online] Available at: https://readthedocs.org/projects/pynq/ [Accessed 23 Oct. 2018].

4. Ieeexplore.ieee.org. (2018). *Commissioning and testing of SERENDIP VI instrumentation USNC-URSI national radio science meeting - IEEE Conference Publication*. [online] Available at: https://ieeexplore.ieee.org/document/7436240/ [Accessed 23 Oct. 2018].

5. GitHub. (2018). *casper-astro/mlib_devel*. [online] Available at: https://github.com/casper-astro/mlib_devel/blob/6904b15a79ecfc00656d77bd3d36b47958e452fb/CODE_OF_CONDUCT.md [Accessed 25 Oct. 2018].

6. "Safety • Electrical and Computer Engineering • Iowa State University", *Ece.iastate.edu*, 2018. [Online]. Available: https://www.ece.iastate.edu/the-department/safety/. [Accessed: 25- Oct- 2018]

7. IEEE Std 211-1997™ IEEE Standard Definitions of Terms for Radio Wave Propagation

8. IEEE Std 1241-2010™ IEEE Standard of Terminology and Test Methods for Analog-to Digital Converters

9. IEEE Std 802.3™ Standards for Ethernet

10. W. New, "JASPER and the SKARAB", 2017 CASPER Workshop, California Institute of Technology, 2017.

11. L. Shu, "SNAP2's development toolflow and applications", 2018 CASPER Workshop, Guizhou Province, China, 2018.

12. Xilinx.com. (2018). [online] Available at: https://www.xilinx.com/support/documentation/application_notes/xapp1305-ps-pl-based-ethernet-solution.pdf [Accessed 23 Oct. 2018].

13. Xilinx.com. (2018). *Zynq UltraScale+ RFSoC Data Converter*. [online] Available at: https://www.xilinx.com/support/documentation/ip_documentation/usp_rf_data_converter/v2_0/pg269-rf-data-converter.pdf [Accessed 23 Oct. 2018].

14. Price, D. (2018). Spectrometers and Polyphase Filterbanks in Radio Astronomy. [online] Arxiv.org. Available at: https://arxiv.org/abs/1607.03579 [Accessed 23 Oct. 2018].