sdmay19-41: Wideband Full Stokes parameterised spectrometer for Xilinx RFSoc Platform

Week 2 Report
September 17 - September 25

Team Members

Brian Bradford — *DSP Engineer and Meeting Facilitator*
Niki-Louis Hamilton — *FPGA Engineer and Meeting Scribe*
Jared Danner — *FPGA Engineer and Report Manager*
Nicholas Knuth — *FPGA Engineer*
Vishal Joel — *GUI Developer and FPGA Engineer*

Summary of Progress this Report

Researched the PYNQ libraries already developed for the Xilinx RFSoC Evaluation Board. Met w/ client (discussed the architecture of CASPER's Toolflow) and our adviser. The team collectively investigated Vivado to familiarize ourselves and have started downloading/install Migen.

Pending Issues

Migen tcl script generation may not suffice for Vivado. Need Xilinx board to run through tutorials. We also are still unsure of what is already developed and what is not for the board support package.

Plans for Upcoming Reporting Period

Get our hands on the Xilinx board and run through the tutorials supplied by Xilinx. Narrow down what is unsupported for the Xilinx ZCU106 platform.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Brian Bradford	Currently in China networking w/ CASPER engineers.	7	15
Niki-Louis Hamilton	Tutorials on Migen and installed Jupyter Notebook.	8	16
Jared Danner	Cloned down and started researching through what is support via PYNQ. Reached out to advisers regarding tools, report templates, when the board will arrive.	7.5	15.5
Nicholas Knuth	Started looking at Vivado and finding simple tutorials to start working on to familiarize the team with Vivado. Looked into installing Migen and seeing what is already supported on the board we are using.	8	16

Vishal Joel	I went through the migen documents, and familiarized myself with the basic use of the program. I also went through vavado's example projects to get a basic idea of how the program works.	7	15

Gitlab Activity Summary

Nothing to report.