EE CprE 491 – May 1819
sdmay19-41 Senior Design Team
Week 7 Report

September 25 - October 1
Faculty Advisors: Phillip Jones

Team Members:

Brian Bradford — *DSP Engineer and Meeting Facilitator*
Louis Hamilton — *FPGA Engineer and Meeting Scribe*
Jared Danner — *FPGA Engineer and Report Manager*
Nick Knuth — *FPGA Engineer*
Vishal Joel — *GUI Developer and FPGA Engineer*

Summary for Progress this Week

This past week our group met with our faculty advisor and discussed the direction that the team should take due to not having the appropriate hardware to proceed with the Vivado and ZYNQ tutorials. The team then proceeded to successfully complete one of the start up guides on how to walk through the creation of a Vivado project including the generation of the bitstream and the physical gate design that the FPGA is using.

Past Week Accomplishments

- Completion of a Vivado Quick Start Guide for the Zynq UltraScale+ MPSoC FPGA
    - Experienced how to create a basic project.
    - Worked through the basic project flow in Vivado
    - Familiarized ourselves with the user interface of Vivado
    - Worked through the structure of a Vivado project and what each step results in
- Worked through Lab 1 of CPRE 488
    - Read the overview and background information
    - Understood the goal of this lab and the design of an FPGA
    - Completed as much of the lab as possible without a board
- Attended annual CASPER conference that was in China (Brian)
    - Discussed alternative front-ends to existing toolflow (removing MATLAB dependency)
    - Brainstormed easiest way to support Zynq platform with existing tools
    - Discussed adapting backend to target different FPGA platforms using Migen or MyHDL
    - Developers agreed to standardize on AXI interfaces instead of Wishbone
    - Brainstormed best way to support unit testing in toolflow: Vunit, Migen, and MyHDL
    - Spoke with different Institutions/groups about wanted support for the RFSoC

Pending Issues

Current Vivado installation on linux servers does not have System Generator support, which must be included in order to run the current CASPER Toolflow.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Brian Bradford	Attended annual CASPER conference in China	10	25
Louis Hamilton	Vivado setup tutorials search and Linux driver research	4	20
Jared Danner	PYNQ & Migen interaction. Researched Wishbone. Vivado / Matlab tutorials.	5	20.5
Nick Knuth	Vivado/Matlab tutorials	4	20
Vishal Joel	Vivado/Matlab tutorials and videos	4	19

Comments and Extended Discussion

Brian talked about what happened at the CASPER conference.

Plans for Coming Week

Complete a simple implementation with Migen. Reach out about status of boards. Update senior design website. Contact ETG about not fully installing Vivado: System Generator and DocNav. Work through existing CASPER tool flow tutorial.

Summary of Weekly Advisor Meeting

This past week our group met with our faculty advisor and discussed the direction that the team should take due to not having the appropriate hardware to proceed with the Vivado and ZYNQ tutorials. He suggested completing the initial lab offered by Xilinx for their boards. We were unable to access the tutorials on our laptops. He suggested different ways to access the documentation online and we eventually were able to open the documentation in the TLA. He also asked us to contact ETG about the problem to fix the configuration issue with the document navigation in Vivado. He also suggested going through and replicating the Xilinx tutorial in Migen.

Minutes

- We spoke to Dr. Jones about an issue that arose with accessing the linux remotes servers (We had no visual GUI).

    - **Solution :** Use the Windows Remote Desktop application.
- We also received the Status Report template that Dr. Jones wanted us to use from here on.
- We began work on the tutorials present in Vivado.
    - Initially we had issues with accessing the tutorial documentation present in the Vivado.
        - Note: The documentation can be accessed using the TLA linux computers, the computers in Coover 2048 or remote desktop cannot access the documentation.
        - An Email needs to be sent to ETG to fix the above issue.
    - Using the the TLA linux computers we started “Vivado Design Suite Tutorial: Embedded Processor Hardware Design (UG940)”.
        - Lab 1 was completed : Building a Zynq Ultrascale+ MPSoC Processor Design. It was a simple I/O interface. Test was successful.
- Prepare for meeting tomorrow with Alan.