EE CprE 491 – May 1819
sdmay19-41 Senior Design Team
Week 9 Report

October 9 - October 16
Faculty Advisors: Phillip Jones

Team Members:

Brian Bradford — *DSP Engineer and Meeting Facilitator*
Louis Hamilton — *FPGA Engineer and Meeting Scribe*
Jared Danner — *FPGA Engineer and Report Manager*
Nick Knuth — *FPGA Engineer*
Vishal Joel — *GUI Developer and FPGA Engineer*

Summary for Progress this Week

This past week we finished up the first iteration of the Design Document and we went into great detail about the functional block diagrams concerning the Xilinx ZCU111 RFSoC UltraScale+ and the CASPER ToolFlow. Diving into the system diagrams allowed us to get a good understanding of the components we will be working with. By separating each subsystem, we were able to assign specialty areas to members and therefore allow each individual to start progressing on their own.

Past Week Accomplishments

- Fixed Issues:
    - Dr. Zambreno / ETG installed Xilinx System Generator for Vivado 2018.2
    - Updated Senior Design Website to reflect latest work (Weekly Status report and Design Document)
- Documentation - All group members
    - Finished first iteration of Design Document.
    - Created functional block diagrams of the systems we will be working with.
- Researched ZCU111 ADCs - Jared Danner
    - Familiarized self with what an FMC was and how they are used.
    - The ZCU111 uses a FPGA Mezzanine Card (FMC) for ADC support.
        - Model of FMC: XM500 RFMC Balun Add-on Card
            - Onboard ADCs (RFMC & ADC) / DACs
                - RFMC : Specialized radio frequency ADCs
                - ADC: Normal Analog to Digital
        - ZCU111 supports VITA v57.4 FMC+
            - VITA being an organization who creates critical high speed embedded system components.
- Research PYNQ overlay creation - Brian Bradford/Nick Knuth

    - Read through docs trying to understand the PYNQ architecture and APIs: https://pynq.readthedocs.io/en/latest/index.html
    - Trying to understand PYNQ, Migen, and existing CASPER toolflow integrations
    - Petalinux BSP install
- Hands-on with PYNQ-Z1 board (Joel and Louis)
    - Reading through the setup documentations and setting up the PYNQ-Z1 board. (https://pynq.readthedocs.io/en/v2.0/getting_started.html)
    - Going through the Jupyter Notebooks documentations and trying to understand how it works using the samples provided in the interactive computer environment. We went through the live code, such as reading and writing from the ADC, plotting the read data, etc.
    - Learned about the PYNQ-Z1 board and its hardware features.
- Created GitLab submodules for existing CASPER toolflow repo and PYNQ repo (Brian)

Pending Issues

Need to verify System Generator/DocNav functionality for Vivado 2018.2.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Brian Bradford	Design Document, Diagrams, researched PYNQ overlay creation, and GitLab submodules	6	37
Louis Hamilton	Researching how to develop on the PYNQ Z1 in preparation for using the ZCU106 with PYNQ.	7	32
Jared Danner	Researched the XM500 RFMC ADC riser attachment to the ZCU111. Ran through PYNQ tutorial w/ large group. Started a PYNQ tutorial through Jupyter Notebook for the ZCU106 ADC.	5	32
Nick Knuth	Documentation and Research PYNQ and Linux on Xilinx boards	6	32
Vishal Joel	Documentation, and Research with PYNQ Z1. Also running and understanding the examples provided in Jupyter Notebooks.	6	30.5

Comments and Extended Discussion

Plans for Coming Week

Play with PYNQ-Z1 board to understand functionality better. Start adding PYNQ support of ZCU106, based on ZCU104 overlays. Determine integration for PYNQ, Migen, and existing CASPER toolflow.

Summary of Weekly Advisor Meeting

This past week our group met with our faculty advisor and discussed issue fixes and verification from previous week. Checked out the PYNQ-Z1 board to familiarize team with PYNQ functionality.

Minutes

- Checked out PYNQ-Z1 board.
- Started working with the board, researching development of a custom overlay for the board.
- Discussed / verified System Generator and DocNav installation.
- We completed the first iteration of the Design Document.