# EE CprE 491 – May 1819
# sdmay19-41 Senior Design Team
# Week 10 Report

*October 17 - October 25*
*Faculty Advisors: Phillip Jones*

## Team Members:

Brian Bradford — *DSP Engineer and Meeting Facilitator*
Louis Hamilton — *FPGA Engineer and Meeting Scribe*
Jared Danner — *FPGA Engineer and Report Manager*
Nick Knuth — *FPGA Engineer*
Vishal Joel — *GUI Developer and FPGA Engineer*

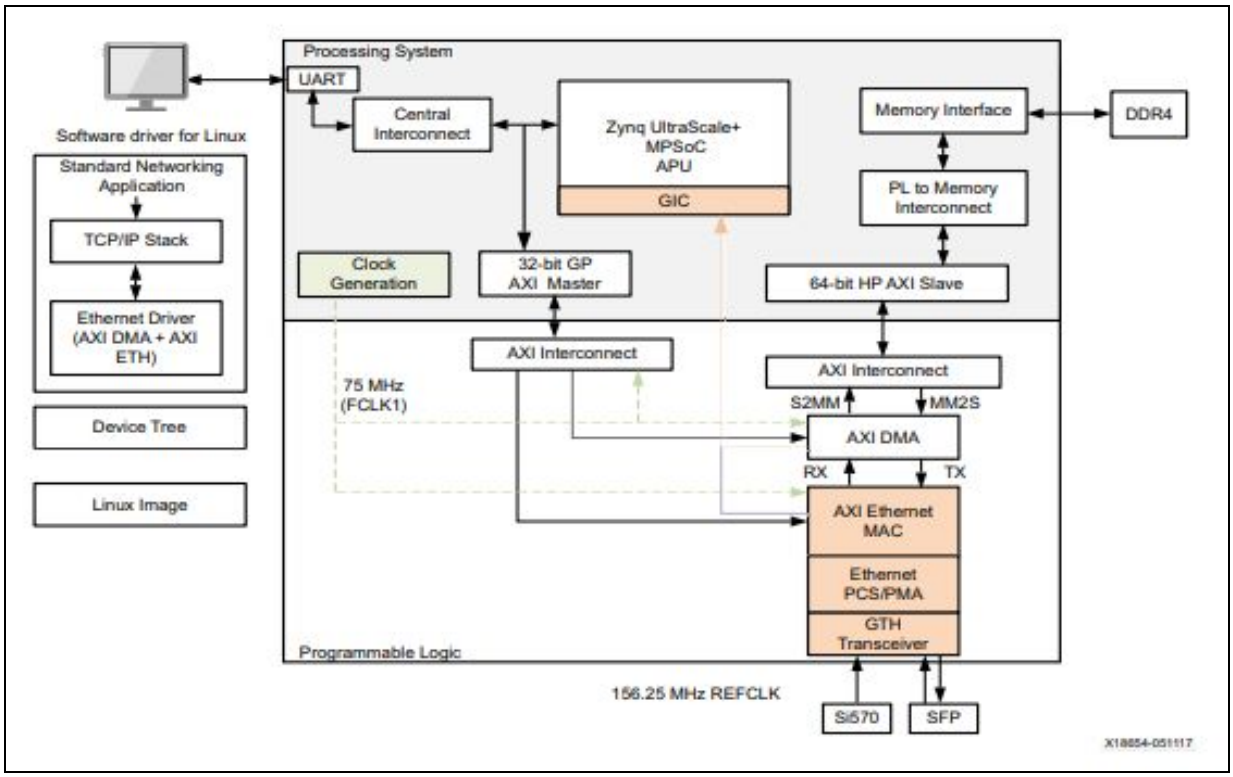
## Summary for Progress this Week

This week saw a major technical hurdle be passed. The MPSoC evaluation kits arrived and our group members have either applied for or received lab access to Coover 3050. As a group we tried to install linux onto the MPSoC in the hopes that linux would handle many of the basic drivers required for our project. The final portion of our week saw the completion of the second iteration of our group's project plan document.

## Past Week Accomplishments

- Fixed Issues:
    - MPSoC Evaluation Kits have arrived.
- Documentation - All group members
    - Finished second iteration of Project Plan.
    - Found more functional block diagrams of the systems that we will be working with.
- Completed Setup Tutorial of MPSoC platform - All members
    - Began the process of flashing the BSP and other necessary files
    - Planned out how linux would interact with the platform
- Began PYNQ support of ZCU106 board based on ZCU104 design
    - Need ETG to run a setup script to work on Linux servers
    - Edited BSP and constraints files
    - Edited ZCU104 python modules to reflect ZCU106

- Xilinx 10Gig Ethernet Block (Seen below)
    - Credit to Xilinx Ethernet IP Core.




## Pending Issues

Waiting for response from ETG concerning the installation of some libraries needed to install PYNQ onto the MPSoC boards.

## Individual Contributions

| Team Member | Contribution | Weekly Hours | Total Hours |
|---|---|---|---|
| Brian Bradford | Xilinx 10GbE hardware design, Project Plan V2, and began ZCU106 PYNQ support | 5 | 42 |
| Louis Hamilton | Yellow Block research (through JASPER toolflow), Project plan V2 | 5.5 | 37.5 |
| Jared Danner | MPSoC Initialization Tutorial / Project Plan Documentation | 5 | 37 |
| Nick Knuth | MPSoC tutorial, Project Plan v2 | 5 | 37 |

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|---|---|---|---|
| Vishal Joel | More research with Jupyter notebooks - local installation to work outside Senior design hours. Project Plan v2 | 5.5 | 36 |

## Comments and Extended Discussion

## Plans for Coming Week

Pending that we hear back from ETG regarding PYNQ library dependencies that required sudo to install, we will be flashing the PYNQ image to the MPSoC which will allow us to truly begin to understand with how PYNQ can interface with the system. Beyond this, we hope to get the Xilinx linux kernel installed onto the board.

## Summary of Weekly Advisor Meeting

This past week our group met with our faculty advisor and discussed how we need to include more technical information in our weekly reports. We confirmed that we received the MPSoC kits and that they were in Coover 3050.

**Minutes**

- Started working with the MPSoC Evaluation Kit. Completed setup tutorial.
- Began the process of flashing PYNQ to the board.
- We completed the second iteration of the Project Plan.
- Gained keycard access to Coover 3050.