EE CprE 491 – May 1819
sdmay19-41 Senior Design Team
Week 12 Report

October 26 - November 6
Faculty Advisors: Phillip Jones

Team Members:

Brian Bradford — *DSP Engineer and Meeting Facilitator*
Louis Hamilton — *FPGA Engineer and Meeting Scribe*
Jared Danner — *FPGA Engineer and Report Manager*
Nick Knuth — *FPGA Engineer*
Vishal Joel — *GUI Developer and FPGA Engineer*

Summary for Progress this Week

These past two weeks were primarily focused on three subjects, 1) deciphering the two directions our group could have taken to implement the ethernet port, 2) finalizing our understanding of how PYNQ will be interfacing with the RFSoC/MPSoC platforms (will use a AXI/Wishbone bus), and 3) figuring out if our group should utilize the quad core arm processor onboard the RFSoC or to use a LWIP microblaze softcore processor in the FPGA's fabric.

Past Week Accomplishments

- Fixed/Pending Issues:
    - Continuing to work w/ ETG to get dependant libraries install that are needed to run PetaLinux.
- Documentation - All group members
    - Created and finalized our group's technical lightning talk.
        - Created & linked functional block diagrams to show the system interaction.
- Began to Implement PetaLinux. - Brian & Nick
    - Ran into issues installing libraries needed to run PetaLinux & PYNQ.
    - Began rewriting the setup script to work on the Iowa State Linux distributions
    - Forked PYNQ repo and began work on rewriting the ZCU104 branch into a ZCU106 branch for our board
- Investigated the depth of Vivado Simulation. - Joel & Jared & Louis
    - Read through & followed tutorials regarding the type of simulations that are possible through the Vivado Design Suite.
- RFSoC ADC - Jared
    - Walked through developer guides with the RFSoC RMFC ADC ports.
    - Accumulated technical knowledge and documentation over the RMFC ADCs.
- Finalized design choices for ethernet
    - RJ45 port will be used to communicate with PetaLinux and configure the board

- SFP port will be used for data throughput
- Initial implementation will aim to be 1GbE for both ports

Pending Issues

Waiting for response from ETG concerning the installation of some libraries needed to install PYNQ onto the MPSoC boards.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Brian Bradford	Ethernet, PetaLinux, Documentation, Github Corrections	8	50
Louis Hamilton	CASPER Tool-flow Yellow Blocks / Compiling overlays onto ZNYQZ1 Board	6	43.5
Jared Danner	ADC RMFC Whitepapers / PYNQ <-> Wishbone / PYNQ Xilinx tutorials	8	45
Nick Knuth	Ethernet, PetaLinux, Documentation	8	45
Vishal Joel	More research with Jupyter notebooks, documentation and vivado simulation	8	44

Comments and Extended Discussion

Plans for Coming Week

The plans for the coming week are to focus on forking over PYNQ to work with the ZCU106 platform from its ZCU104 branch. Beyond this, we are continuing to dive into Vivado's simulation tool set to figure out the depth as to which we can test our designs prior to receiving the official RFSoC Evaluation Kit. Work will continue on integrating the 1 Gigabit ethernet port into the MPSoC platform.

Summary of Weekly Advisor Meeting

This past week we met with our advisor and discussed our progress on the ethernet implementation and the ADC simulation and implementation.

Minutes

- Spoke about the different ways we could go about implementing ethernet communication
- Spoke about the ADC capabilities
- Our advisor suggested looking into simulation capabilities