EE CprE 492 – May 1819
sdmay19-41 Senior Design Team
Weekly Report 1

January 7th - January 31st
Faculty Advisors: Phillip Jones

Team Members:

Brian Bradford — *DSP Engineer and Meeting Facilitator*
Louis Hamilton — *FPGA Engineer and Meeting Scribe*
Jared Danner — *FPGA Engineer and Report Manager*
Nick Knuth — *FPGA Engineer*
Vishal Joel — *GUI Developer and FPGA Engineer*

Summary for Progress this Week

The weeks this report encompasses include our first meetings with both our faculty advisor and our Casper project advisor and individual work by each team member.

Past Week Accomplishments

- Gitlab issue and milestones setup
    - Planned ways to use Gitlab to track sprints on the advice of Alan
    - Added major milestones to Gitlab that we need to complete first
    - Each team member added issues to each milestone to highlight subtasks
- Continued Implementation of 10Gbe - Nick
    - Setup remote desktop view for server to use applications outside of command line with Brian's help
    - Continued to look at current implementation and what needs to change to match ZCU 106 and 111 platforms
- Work during break and first two weeks - Brian
    - Spent a week in Berkeley working on project and consulted with various CASPER members
    - Tweaked a CASPER spectrometer application in Simulink to match our needs, System generated DSP code to be pulled into Migen
    - Started creating skeleton Migen module for the Spectrometer application which exposed all inputs/outputs needing to interface to either ADC, 10 GbE, or software registers
    - Created ZCU106 and ZCU111 PYNQ images
    - Tested/verified ZCU106 PYNQ functionality
    - Ported ZCU104 base overlay to ZCU106 and tested, blinked leds via PYNQ, verified switches/buttons (had to strip out HDMI IP because of license)
    - Investigated Vivado IP/PYNQ equivalent of CASPER software register
    - Assisted Louis and Joel with configuration of VNC to remote into our machine

- ADC Vivado Design - Jared
    - Spent 7 days out at University of California, Berkeley learning from the CASPER team members regarding ADC and FPGA design.
    - Located a Targeted Reference Design Vivado project utilizing the ADCs and DACs in a Multi-Tile Synchronized approach. I am currently in the process of removing the DACs and ZYNQ Processor from the TRD to reduce FPGA PL utilization and unused logic.
    - I am also in process of testing the characterization of the original Multi-Tile Synchronization TRD via a Vivado GUI that has been created specifically for testing this TRD.
    - Spent numerous hours learning the ins and outs of Vivado, how ADCs function at a verilog level, and how to control various IP cores downstream of the ADC IP Driver.
    - Created ADC interface related issues/milestones on Gitlab.
- GNU Radio tools - Joel
    - Resolved all dependency issues in using both GNU Radio tools and its components. Due to the numerous amount of components that GNU Radio tools offers, along with all their respective dependencies the previous installation only allowed the companion tool to work.
    - I am currently in the process of using GNU Radio tools directly as a python module to interface with the Z1.
- Setting the Environment for the ZCU106/111 - Louis
    - Creating a base Overlay with a “Software Control” register, allowing register editing in Jupyter Notebooks.
        - Looking for a possible “Software Register”module already in Vivado, if not it must be created.
    - Using the Overlay from the previous point and adding a 10g interface and a ADC interface.

Pending Issues

None currently. Continuing to work on existing goals.

Individual Contributions

Team Member	Contribution	Weekly Hours	492 Total Hours	Total Hours
Brian Bradford	Gitlab issues and milestones, PYNQ, migen, and Spectrometer app	9	83	157.5
Louis Hamilton	Gitlab issues and milestones, PYNQ, build environment	6	15	81.5

Jared Danner	Gitlab issues and milestones, ADC interface in Vivado, testing Vivado TRD.	7	67	133
Nick Knuth	Gitlab issues and milestones, Continued Implementation of 10Gbe	8.5	8.5	70
Vishal Joel	Gitlab issues and milestones and GNU Radio Tools	7	13	73

Comments and Extended Discussion

Jared - I am currently hitting roadblocks when I try to synthesize the TRD that has the DACs and PS removed. The errors that are occuring are “overlapping memory” in certain IP Cores and High Performance ports. I believe this is due to my inexperience with Vivado Tools and the TRD that I am operating on. I will continue to work on this project as I gain more knowledge of Vivado, but in the meantime, I will pivot to working on the testing of the original Vivado TRD.

Plans for Coming Week

Continue work on milestones and issues on the Gitlab page

Start testing the ADC/DAC TRD with the Vivado given GUI. This will be done by generating a predefined signal/noise out of the DAC and reading that same signal back in through the ADCs at various sampling speeds to better learn what settings will best suite our project’s needs.

Create example project with equivalent of CASPER’s software register block in Vivado and read/write from PYNQ.

Summary of Weekly Advisor Meeting

We met and discussed our current plans for this semester and what each of us will be working on. We also discussed our plans to use gitlab to track our progress on each task and keep our work more organized as we are starting to break up the work much more this semester.

Minutes

- Explained to Dr. Jones what each of us will be doing in the near future
    - Explained moving to a sprint system using Gitlab to track issues and milestones
- He advised us on finding issues early and getting help as quick as possible.
- He also wanted us to make sure that we are prepared to test our components and to develop more concrete testing plans as we go.