EE CprE 492 – May 1819
sdmay19-41 Senior Design Team
Weekly Report 2

February 1st - February 7th
Faculty Advisors: Phillip Jones

Team Members:

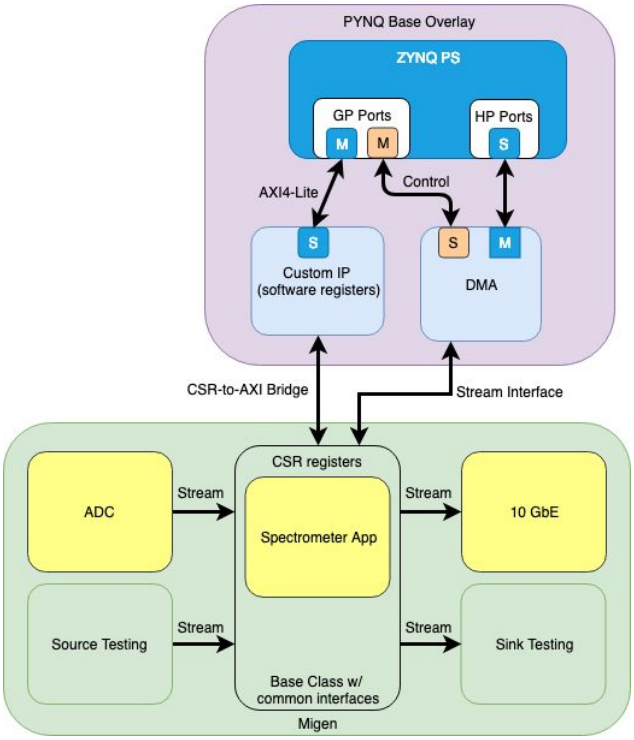
Brian Bradford — *DSP Engineer and Meeting Facilitator*
Louis Hamilton — *FPGA Engineer and Meeting Scribe*
Jared Danner — *FPGA Engineer and Report Manager*
Nick Knuth — *FPGA Engineer*
Vishal Joel — *GUI Developer and FPGA Engineer*

Summary for Progress this Week

This week saw individual work by each of us as well as the start of a working diagram of our final implementation goals.

Past Week Accomplishments

- Gitlab issue and milestones setup
    - Continued to flesh out these issues.
    - Started to set dates to create a concrete timeline of tasks
- Continued Implementation of 10Gbe - Nick
    - Completed first steps of implementation and synthesis.
    - Working on next steps of implementation by correcting some sub components of ported design
    - Begin work on writing a wrapper for the core to make integration and testing easier
- PYNQ Overlays - Brian
    - Tested/verified ZCU111 PYNQ image
    - Ported ZCU104 base overlay to ZCU111 and tested, blinked leds via PYNQ, verified switches/buttons (had to strip out HDMI IP because of license) NOTE: our base overlay will be built around this existing one
    - Theorized how CSR registers from Migen can be accessed via PYNQ
    - Discussed with Alan: Migen CSR-to-AXI bridge, Base Migen module class with common streaming/config interfaces to be inherited by all Modules, possibly of DMA use for system testing.
    - Designed PYNQ overlay for project, drew out high-level system architecture to describe all interfaces and bridging between PYNQ and Migen (See below)
    - Created new Gitlab issues reflecting future work from these designs



- ADC Vivado Design - Jared
    - I am still in the process of testing the characterization of the original Multi-Tile Synchronization TRD via a Vivado GUI that has been created specifically for testing this TRD.
    - Roadblocks have arisen such as the need for LabView (Texas Instrument product) which is a requirement for the ADC Eval GUI to install.
    - Read through many more data sheets concerning the onboard ADCs and how they function at a physical level.
- GNU Radio tools: Research on various data sample reading implementations - Joel
    - Researching on how to use the UDP source block on GNU radio. (simply takes the content of UDP datagrams and puts them into the GR flow graph. The only disadvantage is that you can't control the device or use any particular features beyond the stream of samples).
    - Another possible implementation is using an out of tree source block (if the above method doesn’t work)
- ZCU106/111 - Louis
    - Researched possible Software registers registers that interface with Simulink. A possible PYNQ IP could work for this purpose.

Pending Issues

None currently. Continuing to work on existing goals.

Individual Contributions

Team Member	Contribution	Weekly Hours	492 Total Hours	Total Hours
Brian Bradford	ZCU111 base overlay port/design, system architecture drawing, Gitlab issues	6	89	163.5
Louis Hamilton	Base Overlay research	3	18	84.5
Jared Danner	Continued testing of Vivado ADC TRD.	5.5	72.5	138.5
Nick Knuth	Gitlab issues and milestones, Continued Implementation of 10Gbe	6	14.5	76
Vishal Joel	GNU Radio Tools research on UDP source block	5	18	78

Comments and Extended Discussion

Jared - As mention above, the GUI has turned out to be a program that has required many IP programs to be installed prior (LabView, etc..). This process has slowed down progress due to Texas Instruments not granting student access to LabView in a timely manner. Customer Support has been contacted.

Plans for Coming Week

Continue work on milestones and issues on the Gitlab page

Initial testing the ADC/DAC TRD with the Vivado given GUI.

Create example project with equivalent of CASPER's software register block in Vivado and read/write from PYNQ.

Summary of Weekly Advisor Meeting

We met and discussed our current plans for this semester and what each of us will be working on. We also discussed our plans to use gitlab to track our progress on each task and keep our work more organized as we are starting to break up the work much more this semester.

Minutes

- Explained to Dr. Jones what each of us will be doing in the near future
    - Explained moving to a sprint system using Gitlab to track issues and milestones
- He advised us on finding issues early and getting help as quick as possible.
- He also wanted us to make sure that we are prepared to test our components and to develop more concrete testing plans as we go.