EE CprE 492 – May 1819
sdmay19-41 Senior Design Team
Weekly Report 3

February 8th - February 14th
Faculty Advisors: Phillip Jones

Team Members:

Brian Bradford — *DSP Engineer and Meeting Facilitator*
Louis Hamilton — *FPGA Engineer and Meeting Scribe*
Jared Danner — *FPGA Engineer and Report Manager*
Nick Knuth — *FPGA Engineer*
Vishal Joel — *GUI Developer and FPGA Engineer*

Summary for Progress this Week

Continued individual progress on each task we have assigned. Completed presentation slides for our meeting with Dr. Manimaran.

Past Week Accomplishments

- Gitlab issue and milestones setup
    - Continued to flesh out these issues.
    - Set dates and indicated progress on each one
- 1-on-1 Presentation
    - Completed presentation slides for meeting on Friday, February 15th
    - Gathered weekly reports into one file
- Continued Implementation of 10Gbe - Nick
    - Continued work on sub component implementation
    - Began looking at how the interface for the ethernet should be completed
    - Begin work on starting a testbench for the ethernet to test independently of the whole project.
- PYNQ Overlays - Brian
    - Began created Base Overlay based on Interface Architecture drawing from last week
    - Brought base overlay wrapper from Vivado into Migen (pynq_overlay Migen module)
    - Began creation of BaseModule for all Migen project modules to inherit from with common configuration and streaming interfaces
    - Hooking up test CSR registers with AXI4-Lite to CSR bridge to verify functionality from PYNQ
- ADC Vivado Design - Jared
    - Waiting for ETG to install dedicated Windows machine with necessary tools and privileges to use the Xilinx provided GUI for interfacing with the ADCs.

    - Building a 1 channel ADC stream to better learn how components work without the complexity of the entire 8 DACS & 8 ADCs design.
    - As I progress in my understanding from conducting the above bullet point, I am continuing to strip down the Xilinx provided MTS ADC design.
- GNU Radio tools: Research on various data sample reading implementations - Joel
    - Researching on how to use the UDP source block on GNU radio. (simply takes the content of UDP datagrams and puts them into the GR flow graph. The only disadvantage is that you can't control the device or use any particular features beyond the stream of samples).
    - Work with Adalm Pluto SDR (provided by Alan) to get more familiar with working on GNU Radio.
- PYNQ - Louis
    - Created a vivado project using DIrect Memory Access (DMA) IPs to create a streaming interface to test resizing a photo on Jupyter Notebooks.
        - This provides a prototype of sorts to testing working with DMAs for use on the ZCU104/111

Pending Issues

None currently. Continuing to work on existing goals.

Individual Contributions

Team Member	Contribution	Weekly Hours	492 Total Hours	Total Hours
Brian Bradford	Migen base wrapper module, casper base migen module, CSR to AXI test	6	95	169.5
Louis Hamilton	PYNQ-Z1 DMAs	7	25	91.5
Jared Danner	Continued testing of Vivado ADC TRD, 1-on-1 meeting	6	78.5	144.5
Nick Knuth	Gitlab issues and milestones, Continued Implementation of 10Gbe, 1-on-1 meeting	6	20.5	82
Vishal Joel	GNU Radio Tools research on various source blocks, 1-on-1 meeting	4	22	82

Comments and Extended Discussion

Jared - As mentioned above, the GUI has turned out to be a program that has required many IP programs to be installed prior (LabView, etc..). This process has slowed down progress due to

Texas Instruments not granting student access to LabView in a timely manner. Customer Support has been contacted.

Plans for Coming Week

Continue work on milestones and issues on the Gitlab page

Initial testing the ADC/DAC TRD with the Vivado given GUI pending ETG updates.

Continue to iterate on the MTS 8 ADC design.

Verify CSR to AXI bridge through CSR register access from PYNQ.

Summary of Weekly Advisor Meeting

We gave updated status for each of our tasks and what each of us will be working on in the next week. We spoke about general rules to follow in development for FPGA's and project work.

Minutes

- Explained to Dr. Jones what each of us will be doing in the near future
    - Fleshed out sprint system in Gitlab and gave Dr. Jones access
- Advised us on general practice for development
- Advised us to begin testing as soon as we can to find issues and identify them as early as possible