EE CprE 492 – May 1819
sdmay19-41 Senior Design Team
Weekly Report 4

February 15th - February 21st
Faculty Advisors: Phillip Jones

Team Members:

Brian Bradford — *DSP Engineer and Meeting Facilitator*
Louis Hamilton — *FPGA Engineer and Meeting Scribe*
Jared Danner — *FPGA Engineer and Report Manager*
Nick Knuth — *FPGA Engineer*
Vishal Joel — *GUI Developer and FPGA Engineer*

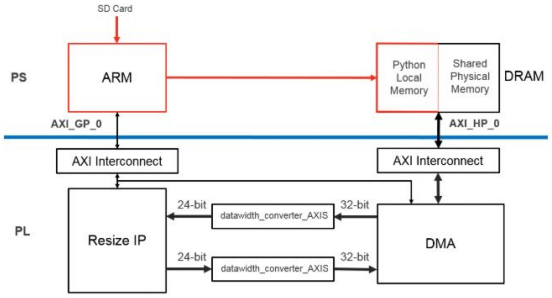
Summary for Progress this Week

Continued existing tasks individually. Held group meeting to update team status

Past Week Accomplishments

- Gitlab issue and milestones setup
    - Continued to flesh out these issues.
    - Indicated progress through comments as progress is made
- Continued Implementation of 10Gbe - Nick
    - Discovered while trying to build for the board that we do not have access to the necessary Xilinx IP core for the design we were porting. Made the decision to lower the speed of the ethernet to 1G as we do have access to the necessary IP core
    - Started build process of 1G ethernet implementation
    - Continued to look at how a wrapper for the block would need to be constructed
- PYNQ Overlays - Brian
    - Finished BaseModule for all Migen project modules to inherit from with common configuration and streaming interfaces
    - Working through Migen test module to test CSR registers with AXI4-Lite to CSR bridge to verify functionality from PYNQ
    - Migen problem with importing Xilinx IP (must be synthesized first) looking at CASPER toolflow to find tcl commands to import IP XCI to project
- ADC Vivado Design - Jared
    - ETG has provided the computer requested. GUI testing can move forward.
    - Building a 1 channel ADC stream to better learn how components work without the complexity of the entire 8 DACS & 8 ADCs design.
    - Continuing to strip out components such as DACs, dma core, and other various IP to reduce unnecessary resource consumption.
- GNU Radio tools: Research on various data sample reading implementations - Joel

    - Researching on using out of tree source block - Still a work in progress (This method gets a thread of its own in which it can do whatever is necessary to obtain samples from the hardware.The UDP source block seems like a better idea at the moment)
    - Work with Adalm Pluto SDR (provided by Alan) to get more familiar with working on GNU Radio.
    - Testing out various sample GNU radio programs using the GNU Radio Wiki to get a better understanding on how to use the GNU Radio companion for analyzing data samples that does not rely on the companion. Successfully ran GNURadio tools directly from python to accept user input by a pipe or forward to modify default frequency/sample rate in a frequency sink.
- PYNQ - Louis
    - Created two Vivado projects that are imported as PYNQ Overlays that allow data processing using the Vivado design:
        - Image Resizer - that interfaces with DRAM through a AXI interconnect to a Direct Memory Access (DMA) IP. This is useful due to the need for a way to stream data from DRAM straight to the Spectrometer for testing.



        - A Finite Impulse response (FIR) filter. The filter uses a streaming interface to connect to the DMA which is connected to DRAM. The plan is to do a similar implementation using a Spectrometer in place of the FIR filter.

Pending Issues

None currently. Continuing to work on existing goals.

Individual Contributions

Team Member	Contribution	Weekly Hours	492 Total Hours	Total Hours
Brian Bradford	Migen CSR to AXI test, Migen Xilinx IP issue	6	101	175.5
Louis Hamilton	PYNQ-Z1 Image Resizer and FIR filter	10	35	101.5
Jared Danner	Successful synthesis of stripped down TRD. Working on implementation issues.	9	87.5	153.5
Nick Knuth	Gitlab issues and milestones, Continued Implementation of 10Gbe	6	26.5	88
Vishal Joel	GNU Radio Tools research on various source blocks	4	26	88

Comments and Extended Discussion

Jared - ETG's provided windows computer has no peripherals. This isn't an issue, but is an annoyance and might slow down progress when I need to "borrow" the monitors, keyboard, and mouse from our linux machine for the duration of testing.

Plans for Coming Week

Continue work and status updates on milestones and issues on the Gitlab page

Finish the stripped down MTS 8 ADC design.

Verify CSR to AXI bridge through CSR register access from PYNQ.

Complete implementation of 1G ethernet and begin testing

Summary of Weekly Advisor Meeting

Discussed project with Dr. Govindarasu for 492. Did not meet with regular advisor.