EE CprE 492 – May 1819
sdmay19-41 Senior Design Team
Weekly Report 5

February 22nd - February 28th
Faculty Advisors: Phillip Jones

Team Members:

Brian Bradford — *DSP Engineer and Meeting Facilitator*
Louis Hamilton — *FPGA Engineer and Meeting Scribe*
Jared Danner — *FPGA Engineer and Report Manager*
Nick Knuth — *FPGA Engineer*
Vishal Joel — *GUI Developer and FPGA Engineer*

Summary for Progress this Week

Continued existing tasks individually. Held group meeting to update team status

Past Week Accomplishments

- Gitlab issue and milestones setup
    - Continued to flesh out these issues.
    - Indicated progress through comments as progress is made
- Implementation of 1Gbe - Nick
    - Continued to try and implement a 1Gbe ethernet core based on example projects from both Casper and Xilinx
    - Made a list of available components and what Casper needs for implementation and how I can change the example project to work
    - Began process of looking into obtaining the 10Gbe ip core from xilinx
- Migen/PYNQ build environment - Brian
    - Still working through Migen test module to test CSR registers with AXI4-Lite to CSR bridge to verify functionality from PYNQ
    - Fixing problems with multiple clock domains in Migen
    - Fixed Migen import Xilinx IP issues
    - Ran into problem where PYNQ must have a block design to be exported as this is where it make pythonic attributes from IP's, however Migen approach is all RTL
    - Crowbarred fix for above problem by tricking Vivado to import existing block design from PYNQ overlay and regenerating targets (via TCL scripts)
- ADC Vivado Design - Jared
    - Finished removing all of the DAC's, DMA, and processing system components from the original Targeted Reference Design. Synthesis is successful.

    - Started to use PYNQ to interface with the newly created adc design. This will allow register configuration and data streaming which will help test the vivado adc design.
- GNU Radio tools - VIshal Joel
    - Currently working on an interface with Louis to communicate with the z1 board. This is a TCP server that will accept packets from the Z1 and use the data acquired to be processed with GNU Radio. Currently in its initial stages.
- PYNQ - Louis
    - Researched testing methods with Direct Memory Access (DMA) in python. The tests involve passing the data into the DMA's input channels and viewing the data that comes through its output channel. Since the FIR filter from the previous week basically did this, it provided a perfect template for test code.

Pending Issues

None currently. Continuing to work on existing goals.

Individual Contributions

Team Member	Contribution	Weekly Hours	492 Total Hours	Total Hours
Brian Bradford	Migen/PYNQ build environment: fixing a lot of issues	10	111	185.5
Louis Hamilton	PYNQ-Z1 DMA Testing Research	9	34	110.5
Jared Danner	Successful synthesis of stripped down TRD. Started to interface w/ PYNQ.	8	95.5	161.5
Nick Knuth	Gitlab issues and milestones, Implementation of 1Gbe	6	32.5	94
Vishal Joel	GNU Radio Tools research on various source blocks	4	30	92

Comments and Extended Discussion

Plans for Coming Week

Continue work and status updates on milestones and issues on the Gitlab page

Start to build a PYNQ overlay to interface with the Vivado ADC design.

Verify CSR to AXI bridge through CSR register access from PYNQ (can actually do this now after numerous unforeseen issues with Migen/PYNQ).

Need to put together calculations relating to throughput of system and various parameters for ADCs and spectrometer application, and to verify that 1 GbE will be sufficient.

Complete implementation of 1G ethernet and begin testing.

Begin work on GNU and PYNQ interface.

Summary of Weekly Advisor Meeting

Discussed pivoting from 10 GbE to 1 GbE core because of licensing issues.