EE CprE 492 – May 1819
sdmay19-41 Senior Design Team
Weekly Report 6

March 1st - March 7th
Faculty Advisors: Phillip Jones

Team Members:

Brian Bradford — *DSP Engineer and Meeting Facilitator*
Louis Hamilton — *FPGA Engineer and Meeting Scribe*
Jared Danner — *FPGA Engineer and Report Manager*
Nick Knuth — *FPGA Engineer*
Vishal Joel — *GUI Developer and FPGA Engineer*

Summary for Progress this Week

Continued existing tasks individually. Held group meeting to update team status

Past Week Accomplishments

- Gitlab issue and milestones setup
    - Continued to flesh out these issues.
    - Indicated progress through comments as progress is made
- Implementation of 1Gbe - Nick
    - Continued to try and implement a 1Gbe ethernet core based on example projects from both Casper and Xilinx
- Migen/PYNQ build environment - Brian
    - Still working through Migen test module to test CSR registers with AXI4-Lite to CSR bridge to verify functionality from PYNQ
    - First test on board failed, investigating proper way to export CSR map from migen to then parse automatically in PYNQ
    - Came across new PYNQ memory map code that might help...
    - Found partial example online of someone accessing CSR map from linux on a Zynq, reached out to him hoping for some example code (Litex contributor)
- ADC Vivado Design - Jared
    - Replicating a similar project (https://github.com/strath-sdr/rfsoc_qpsk) to develop and understanding of how PYNQ will interact with the ADC onboard the RFSoC.
- GNU Radio tools - Vishal Joel
    - Currently working on an interface with Louis to communicate with the z1 board. This is a TCP server that will accept packets from the Z1 and use the data acquired to be processed with GNU Radio. Currently in its initial stages.
- PYNQ/GNU Radio - Louis

- Installed GNU Radio to begin the process of connecting GNU radio with PYNQ. The idea being that through a python class data from the DMAs can be accessed. Communication with Joel's TCP server is in progress.

Pending Issues

None currently. Continuing to work on existing goals.

Individual Contributions

Team Member	Contribution	Weekly Hours	492 Total Hours	Total Hours
Brian Bradford	Migen/PYNQ build environment: fixing a lot of issues	6	117	191.5
Louis Hamilton	PYNQ-Z1 DMA Testing Research	4	38	114.5
Jared Danner	Started to interface w/ PYNQ.	2	97.5	163.5
Nick Knuth	Gitlab issues and milestones, Implementation of 1Gbe	3	35.5	97
Vishal Joel	GNU Radio Tools research on various source blocks	4	30	92

Comments and Extended Discussion

Plans for Coming Week

Continue work and status updates on milestones and issues on the Gitlab page

Deploy a similar PYNQ/RFSoC project to learn how to better create a PYNQ overlay to interface with the Vivado ADC design.

Investigate issue with CSR to AXI bridge through CSR register access from PYNQ (can actually do this now after numerous unforeseen issues with Migen/PYNQ).

Need to put together calculations relating to throughput of system and various parameters for ADCs and spectrometer application, and to verify that 1 GbE will be sufficient.

Complete implementation of 1G ethernet and begin testing.

Begin work on GNU and PYNQ interface.

Summary of Weekly Advisor Meeting

Discussed pivoting from 10 GbE to 1 GbE core because of licensing issues.