# EE CprE 492 – May 1819
# sdmay19-41 Senior Design Team
# Weekly Report 7

*March 8th - April 4th*
*Faculty Advisors: Phillip Jones*

## Team Members:

Brian Bradford — *DSP Engineer and Meeting Facilitator*
Louis Hamilton — *FPGA Engineer and Meeting Scribe*
Jared Danner — *FPGA Engineer and Report Manager*
Nick Knuth — *FPGA Engineer*
Vishal Joel — *GUI Developer and FPGA Engineer*

## Summary for Progress this Week

Continued existing tasks individually. Held group meeting to update team status

## Past Week Accomplishments

- Gitlab issue and milestones setup
    - Continued to flesh out these issues.
    - Indicated progress through comments as progress is made
- Implementation of 1Gbe - Nick
    - Continued implementation and testing of a 1Gbe ethernet core based on example projects from both Casper and Xilinx
    - Build out both an implementation with and without a microblaze core
    - Work on making sure it can be properly integrated with base project design
- Migen/PYNQ build environment and Spectrometer Design/Implementation- Brian
    - Implemented, tested, and verified Migen/Litex CSR-to-AXI bridge by creating a test application with various registers and read/write to them via PYNQ
    - Created PYNQ function that will inherit DefaultIP class to have common attributes as Xilinx IP in PYNQ, this function will parse my CSR register map and define a register map in PYNQ
    - Created Migen wrapper around Matlab/Xilinx system generated HDL with config/status registers: this will have to be tweaked to represent final spec app
    - Working on PYNQ overlay for our application that exposes modules/registers with friendly names (less typing for everyone and shows the power of PYNQ)
    - Made Jupyter notebook based on a past Polyphase Filterbank example that allows me to test/verify parameters of our spectrometer application in Python
    - Talked through an existing Simulink/CASPER toolflow spectrometer application with industry consultant: Jack Hickish
    - Implementing/reworking the existing application to match spectrometer functionality we want and that I tested in the Jupyter notebook

- ADC Vivado Design - Jared
    - Testing ADC configurations via the provided Xilinx Data Converter GUI. This is done using Loopback tests.
    - Configuring our ADC Vivado project to have a sampling frequency of 256 MHz with 2 ADCs providing a total of 100 MHz of bandwidth.
    - Starting to use PYNQ to set internal ADC parameters to needed values.
- GUI - Vishal Joel
    - Exploring other options such as pyplot/bokeh for graph views.
    - Currently working on an interface with Louis to communicate with the z1 board. This is a UDP server that will do server/client communication to send packets.
    - Currently using Jupyter Notebook along with pyplot to plot interactive dummy data samples. (The plan is to use read data from the DMA directly which the server will accept)
- GUI - Louis
    - Created a Jupyter notebook with access to the Z1's DMA and created quick tests for checking the data passed in and out of the Z1's DMA.
    - Integrated a UDP server in the same notebook, that will pass on the data from the Z1's DMA to a client on a seperate Jupyter Notebook. The data is just RAW and unprocessed, and is checked for integrity but not plotted as of yet.
    - Currently working on a Local Area Network server that will work on the Z1 and allow clients on any computer connected to the same LAN to access the Z1 server.

## Pending Issues

None currently. Continuing to work on existing goals.

## Individual Contributions

| Team Member | Contribution | Month Hours | 492 Total Hours | Total Hours |
|---|---|---|---|---|
| Brian Bradford | Migen/PYNQ build environment and Spectrometer design/implementation | 52 | 169 | 243.5 |
| Louis Hamilton | PYNQ-Z1 DMA Testing Research | 25 | 63 | 139.5 |
| Jared Danner | Started to interface w/ PYNQ. Finalizing ADC configuration values and their register offsets. | 33.5 | 131 | 197 |
| Nick Knuth | Gitlab issues and milestones, Implementation of 1Gbe | 31 | 66.5 | 128 |

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|---|---|---|---|---|
| Vishal Joel | Research on Jupyter Notebooks for plotting graphs and managing a UDP server. | 28 | 58 | 120 |

## Comments and Extended Discussion

Need to get in contact with ETG for a 100 MHz Low Pass filter & spectrum analyzer access in 3050. - Jared

## Plans for Coming Week

Continue work and status updates on milestones and issues on the Gitlab page

Verify ADC configuration values on original TRD as well as our teams trimmed down ADC project using a spectrum analyzer & noise generator.

Finalize spectrometer application in Simulink, system generate, and wrap in Migen. Work on Pynq overlay with spectrometer module instantiated and verify register access.

Complete implementation of 1G ethernet and begin testing.

Begin work on ZCU111 GUI

## Summary of Weekly Advisor Meeting

Discussed pivoting from 10 GbE to 1 GbE core because of licensing issues.