EE CprE 492 – May 1819
sdmay19-41 Senior Design Team
Weekly Report 8

April 5th - April 11th
Faculty Advisors: Phillip Jones

Team Members:

Brian Bradford — *DSP Engineer and Meeting Facilitator*
Louis Hamilton — *FPGA Engineer and Meeting Scribe*
Jared Danner — *FPGA Engineer and Report Manager*
Nick Knuth — *FPGA Engineer*
Vishal Joel — *GUI Developer and FPGA Engineer*

Summary for Progress this Week

Continued existing tasks individually. Held group meeting to update team status.

Past Week Accomplishments

- Gitlab issue and milestones setup
    - Continued to flesh out these issues.
    - Indicated progress through comments as progress is made
- Implementation of 1Gbe - Nick
    - Continued implementation and testing of a 1Gbe ethernet core based on example projects from both Casper and Xilinx
    - Build out both an implementation with and without a microblaze core
    - Work on making sure it can be properly integrated with base project design
- Migen/PYNQ build environment and Spectrometer Implementation- Brian
    - Still working on PYNQ overlay for our application that exposes modules/registers with friendly names (less typing for everyone and shows the power of PYNQ)
    - Implementing/reworking the existing application to match spectrometer functionality, specifically adjusting power accumulator and ethernet packet controller to match our data throughput (1 gbe)
    - Assisted Nick with 1 GbE vivado issues from adding existing project cores as RTL modules
- ADC Vivado Design - Jared
    - Reinserting DMA IP cores into Vivado ADC design via the requirement for DMA by the Xilinx Data Converter GUI.
    - Established F_s and other parameters to have 2 ADC channels sampling a 100 MHz spectrum.
    - PYNQ interfacing will take a backseat role until the Vivado ADC design is proven to work.
- GUI - Vishal Joel

    - Currently working on an interface with Louis to communicate with the z1 board. This is a UDP server that will do server/client communication to send packets.
    - Currently using Jupyter Notebook along with pyplot to plot interactive dummy data samples. (The plan is to use read data from the DMA directly which the server will accept)
    - Currently working on a threaded server for accepting multiple connections and sending data to the client.
- GUI - Louis
    - Worked to plot the data transferred to the client from a Server created in a Jupyter notebook.
    - Currently looking into the RFSoC QPSK Transceiver project done by a team at University of Strathclyde. The project uses a ZCU111 includes a Jupyter Notebook with a GUI.
    - Also, created a simple python Server/Client with threading to handle multiple Client requests.

Pending Issues

None currently. Continuing to work on existing goals.

Individual Contributions

Team Member	Contribution	Week Hours	492 Total Hours	Total Hours
Brian Bradford	Migen/PYNQ build environment and Spectrometer design/implementation	4	173	247.5
Louis Hamilton	Server/Client for FPGA to GUI communication	8	71	147.5
Jared Danner	Finalizing ADC configuration values and their register offsets. Reinserted DMA & PS into ADC design.	3	135	200
Nick Knuth	Gitlab issues and milestones, Implementation of 1Gbe	9	75.5	137
Vishal Joel	Research on Jupyter Notebooks for plotting graphs and managing a UDP server.	3	61	123

Comments and Extended Discussion

Plans for Coming Week

Continue work and status updates on milestones and issues on the Gitlab page

Make the Data Converter GUI & our team's ADC design interface via DMA.

Finalize spectrometer application in Simulink, system generate, and wrap in Migen. Work on Pynq overlay with spectrometer module instantiated and verify register access.

Complete implementation of 1G ethernet and begin testing.

Create the a prototype for the Client/Server GUI

Summary of Weekly Advisor Meeting