EE CprE 492 – May 1819
sdmay19-41 Senior Design Team
Weekly Report 9

April 12th - April 18th
Faculty Advisors: Phillip Jones

Team Members:

Brian Bradford — *DSP Engineer and Meeting Facilitator*
Louis Hamilton — *FPGA Engineer and Meeting Scribe*
Jared Danner — *FPGA Engineer and Report Manager*
Nick Knuth — *FPGA Engineer*
Vishal Joel — *GUI Developer and FPGA Engineer*

Summary for Progress this Week

Continued existing tasks individually. Held group meeting to update team status.

Past Week Accomplishments

- Gitlab issue and milestones setup
    - Continued to flesh out these issues.
    - Indicated progress through comments as progress is made
- Implementation of 1Gbe - Nick
    - Continued implementation and testing of a 1Gbe ethernet core based on example projects from both Casper and Xilinx
    - Build out both an implementation with and without a microblaze core
    - Work on making sure it can be properly integrated with base project design
    - Complete setup of environment on server to connect board for testing
- Spectrometer application, 1 GbE help, and PYNQ overlay - Brian
    - Finished spectrometer application and system-generated code, to be wrapped up in Migen module
    - Assisted Nick with 1 GbE vivado project, debugging and transmit example
    - Reworked functional block diagram for poster/reports and drew a well-defined system architecture diagram
    - Still working on PYNQ overlay for our application that exposes modules/registers with friendly names (less typing for everyone and shows the power of PYNQ)
- ADC Vivado Design - Jared
    - Reinserting DMA IP cores into Vivado ADC design via the requirement for DMA by the Xilinx Data Converter GUI.
    - Working on a pink script/overlay to configure the ADC design. This will be done via writing wanted parameter values to specific memory registers.
- GUI - Vishal Joel

    - Work on GUI config handling (parsing JSON files, and creating them to save configs that should be sent to the client via Python server)
    - Using Jupyter's widgets to make changes to config.
- GUI - Louis
    - Created a Server/Client for communication between the ZYNQ PS and the Jupyter Notebooks server, transferring data between any clients connected to a socket on the local LAN.
    - Currently working on a testing verification of data, by testing the config settings for software registers can change based on input.

Pending Issues

None currently. Continuing to work on existing goals.

Individual Contributions

Team Member	Contribution	Week Hours	492 Total Hours	Total Hours
Brian Bradford	Spectrometer design/implementation, 1 GbE assistance, diagrams, PYNQ base Overlay	8	181	255.5
Louis Hamilton	Server/Client for FPGA to GUI communication	9	80	156.5
Jared Danner	Finalizing ADC register offsets. Configuring design with PYNQ.	4	139	204
Nick Knuth	Gitlab issues and milestones, Implementation of 1Gbe	14.5	89.5	151.5
Vishal Joel	GUI config work using Jupyter widget's and JSON.	5	66	129

Comments and Extended Discussion

Plans for Coming Week

Continue work and status updates on milestones and issues on the Gitlab page.

Complete design document and other paperwork.

Finish PYNQ script to configure ADC.

Finalize spectrometer application in Simulink, system generate, and wrap in Migen.

Wrap spectrometer application in Migen module. Verify Pynq overlay with spectrometer module instantiated and register access.

Complete implementation of 1G ethernet and begin testing.

Create the a prototype for the Client/Server GUI.

Summary of Weekly Advisor Meeting